Active Voltage Control of Series Connected IGBTs

Tee Chong Lim
B.Eng. (Hons)

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HERIOT-WATT UNIVERSITY
SCHOOL OF ENGINEERING AND PHYSICAL SCIENCES
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ABSTRACT

Direct series connections of IGBTs allows power device circuits to be utilised at voltages above individual device voltage ratings. Series connected IGBTs require voltage balancing during dynamic and static periods. Static voltage balancing can be achieved with a simple resistive network across each device. Dynamic voltage sharing can be affected through techniques involving either load side control or gate side control. Load side control uses passive elements or auxiliary control circuitry to ensure dynamic voltage sharing between devices. Gate side control involves active modification of the gate drive signal to ensure dynamic voltage sharing.

This thesis focuses on active voltage control, based on gate side control, that forces the IGBT $dV_{ce}/dt$ to follow a pre-determined reference signal, thereby balancing the dynamic voltage across each series connected IGBT. The active voltage control uses a digital approach that facilitates variation of IGBT $dV_{ce}/dt$ during switching therein minimising the additional switching loss normally incurred with the technique. In addition, active clamping of series connected free-wheel diodes during reverse recovery is investigated.

The research presented in this thesis focuses on increased active voltage control functionality and its extension to bridge leg applications. These control features have been investigated at reduced voltage and current levels.
ACKNOWLEDGEMENT

Many people have contributed to my education through their patience, guidance, and support during my post-graduate study at Heriot-Watt University. I especially wish to thank my supervisors Dr. S.J. Finney and Prof. B.W. Williams for their suggestions and ideas on my PhD research.

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<td>$A_{\text{eff}}$</td>
<td>effective area</td>
<td>cm$^2$</td>
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<td>$C$</td>
<td>capacitor</td>
<td>F</td>
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<tr>
<td>$C_{\text{gc}}$</td>
<td>IGBT gate-collector capacitance</td>
<td>F</td>
</tr>
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<td>$C_{\text{in}}, C_{\text{iss}}$</td>
<td>IGBT input capacitance</td>
<td>F</td>
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<td>$C_{\text{M}}$</td>
<td>external Miller capacitance</td>
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<td>doping concentration</td>
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<td>$q$</td>
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<td>static balancing resistor</td>
<td>Ω</td>
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<td>$T_c$</td>
<td>device case temperature</td>
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<td>$t_{DAC}$</td>
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<td>$t_{d(off)}$</td>
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<td>$t_{d(on)}$</td>
<td>IGBT turn-on delay time</td>
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<td>$t_R$</td>
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<td>$t_{fV}$</td>
<td>IGBT collector voltage fall time</td>
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<tr>
<td>$t_{ox}$</td>
<td>gate oxide thickness</td>
<td>cm</td>
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<tr>
<td>$t_{pd(LH)}$</td>
<td>propagation delay from low to high state</td>
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<tr>
<td>$t_{pd(HL)}$</td>
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<td>$t_{RI}$</td>
<td>IGBT collector current rise time</td>
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<td>$t_{RV}$</td>
<td>IGBT collector voltage rise time</td>
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<td>$t_{sc}$</td>
<td>short-circuit withstand time</td>
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<tr>
<td>$V$</td>
<td>voltage</td>
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<td>$V_A$</td>
<td>LED voltage drop</td>
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<td>$V_{an}$</td>
<td>MLI output voltage</td>
<td>V</td>
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<tr>
<td>$V_{ce}$</td>
<td>IGBT collector-emitter voltage</td>
<td>V</td>
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<tr>
<td>$V_D$</td>
<td>static voltage drop</td>
<td>V</td>
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<tr>
<td>$V_{fd}$</td>
<td>feedback collector voltage</td>
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<tr>
<td>$V_g$</td>
<td>gate voltage</td>
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<tr>
<td>$V_{ge}$</td>
<td>IGBT gate-emitter voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ge(th)}$</td>
<td>IGBT turn-on threshold gate voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>differential amplifier output voltage</td>
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<tr>
<td>$V_R$</td>
<td>FWD reverse recovery voltage</td>
<td>V</td>
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<tr>
<td>$V_{ref}$</td>
<td>pre-determined reference voltage</td>
<td>V</td>
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<tr>
<td>$V_s$, $V_{dc}$</td>
<td>DC supply voltage</td>
<td>V</td>
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<td>$\Delta I_L$</td>
<td>difference in device off-state leakage current</td>
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<td>$\Delta I_T$</td>
<td>IGBT tail current difference</td>
<td>A</td>
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<tr>
<td>$\Delta Q$</td>
<td>difference in stored charge</td>
<td>C</td>
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<td>s</td>
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<tr>
<td>$\Delta T$</td>
<td>temperature difference</td>
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<td>$\Delta V$</td>
<td>voltage difference</td>
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- average
- maximum
- minimum
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<tr>
<td>AC</td>
<td>alternating current</td>
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<tr>
<td>ADC</td>
<td>analogue to digital converter</td>
</tr>
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<td>AVC</td>
<td>active voltage control</td>
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<tr>
<td>BJT</td>
<td>bipolar junction transistor</td>
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<tr>
<td>BTB</td>
<td>back-to-back</td>
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<tr>
<td>DAC</td>
<td>digital to analogue converter</td>
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<tr>
<td>DC</td>
<td>direct current</td>
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<tr>
<td>DC-MLI</td>
<td>diode clamped multi-level inverter</td>
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<tr>
<td>DSP</td>
<td>digital signal processor</td>
</tr>
<tr>
<td>DVR</td>
<td>dynamic voltage restorer</td>
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<tr>
<td>EMI</td>
<td>electromagnetic interference</td>
</tr>
<tr>
<td>EMC</td>
<td>electromagnetic conductance</td>
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<tr>
<td>FACTs</td>
<td>flexible AC transmission system</td>
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<tr>
<td>FCT</td>
<td>field controlled transistor</td>
</tr>
<tr>
<td>FCTh</td>
<td>field controlled thyristor</td>
</tr>
<tr>
<td>FC-MLI</td>
<td>flying capacitor multi-level inverter</td>
</tr>
<tr>
<td>FPGA</td>
<td>field programmable gate array</td>
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<tr>
<td>FWD</td>
<td>free-wheel diode</td>
</tr>
<tr>
<td>GaN</td>
<td>gallium nitride</td>
</tr>
<tr>
<td>GTO</td>
<td>gate turn-off thyristor</td>
</tr>
<tr>
<td>HVAC</td>
<td>high-voltage AC</td>
</tr>
<tr>
<td>HVDC</td>
<td>high-voltage DC</td>
</tr>
<tr>
<td>ICH-MLI</td>
<td>isolated cascaded H-bridge multi-level inverter</td>
</tr>
<tr>
<td>IGBT</td>
<td>insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IGCT</td>
<td>integrated gate-commutated thyristor</td>
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<td>Abbreviation</td>
<td>Definition</td>
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<td>JFET</td>
<td>junction field effect transistor</td>
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<tr>
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<td>light emitting diode</td>
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<tr>
<td>MCT</td>
<td>MOS-controlled thyristor</td>
</tr>
<tr>
<td>MLI</td>
<td>multi-level inverter</td>
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<tr>
<td>MOSFET</td>
<td>metal oxide field effect transistor</td>
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<tr>
<td>MTO</td>
<td>MOS turn-off thyristor</td>
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<tr>
<td>MV</td>
<td>medium-voltage</td>
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<tr>
<td>PT</td>
<td>punch through</td>
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<tr>
<td>PWM</td>
<td>pulse width modulation</td>
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<tr>
<td>SCR</td>
<td>silicon controlled rectifier (thyristor)</td>
</tr>
<tr>
<td>Si</td>
<td>silicon-based</td>
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<td>SiC</td>
<td>silicon carbide</td>
</tr>
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<td>static induction transistor</td>
</tr>
<tr>
<td>SITh</td>
<td>static induction thyristor</td>
</tr>
<tr>
<td>SOA</td>
<td>safe operating area</td>
</tr>
<tr>
<td>SMES</td>
<td>superconducting magnetic energy storage</td>
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<tr>
<td>STATCOM</td>
<td>static compensator</td>
</tr>
<tr>
<td>UPFC</td>
<td>unified power flow controller</td>
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<tr>
<td>VARSpeed</td>
<td>variable speed</td>
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<tr>
<td>VHSIC</td>
<td>very high speed integrated circuit</td>
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<tr>
<td>VHDL</td>
<td>VHSIC hardware description language</td>
</tr>
<tr>
<td>VSD</td>
<td>variable speed drive</td>
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PREFACE

Power electronics involving IGBTs has advanced to medium and high voltage applications, where their benefits are cost effective. The main bulk of developments are in the areas of traction and industry, in particular, medium-voltage (2.3kV-6.9kV) variable speed drives. Currently available silicon-based semiconductor power modules (IGCT and IGBT) are limited by device voltage and power ratings. The device voltage rating limitation requires series connection topologies in order to support the system high voltages. This requires addressing of static and dynamic voltage balancing issues.

This thesis focuses on direct series connection of IGBTs, utilising active voltage control (AVC) to achieve dynamic voltage sharing between the series devices. The technique uses the IGBT in the active region in order to achieve transient voltage balance. The methodologies and techniques involved in the series operation of power semiconductor devices for high-voltage, high-power application are presented in eight chapters. Enhancements are proposed to the basic AVC technique, which are demonstrated at reduced voltage and current conditions, in order to achieve reliability and repeatability.

Chapter 1 highlights recent power electronics technology advances and the use of Si power semiconductor devices for medium to high voltage applications. Also discussed is the possibility of alternative device materials (silicon carbide) that may replace Si in future high-power applications.

Chapter 2 investigates the different methodologies, presented in the recent literature, for the development of the medium-voltage, high-power inverter. The relative merits of multi-level inverter (MLI) topologies and series connected power devices, are reviewed. Topologies involving series connection of IGBTs are assessed in Chapter 3. This includes passive and active control methods that have been presented in the recent literature. The former methodology consists of passive elements or auxiliary control circuitry to ensure device dynamic voltage sharing. The latter methodology depends on gate drive linear control techniques to ensure dynamic voltage sharing between devices.

Chapter 4 reviews IGBT gate drive aspects, including enhanced IGBT switching performance and fault protection capabilities.

Chapter 5 presents the proposed active gate drive technique and its design methodology for series IGBT operation. The proposed AVC technique allows the IGBT dVce/dt to follow a pre-determined reference signal, Vref, which is dynamically adjustable.
The experimental results in Chapter 6 show the features and effectiveness of AVC at low voltage and current levels (300Vdc, 20A). Three different IGBT modules (Siemens-BSM75GAL120DN2, Dynex-GP200MHS12, and Mitel-GP600DHB16S) are used in the experiments which illustrate AVC features for two and three series connected IGBTs.

Chapter 7 presents the benefits of AVC on series connected free-wheel diodes (FWDs) during reverse recovery. Common FWD failure is snap recovery during the reverse recovery phase, which causes high-voltage oscillations with excessive voltage overshoot. This chapter illustrates experimentally AVC ability to suppress voltage oscillations and actively clamp excessive voltage overshoot.

Chapter 8, the final chapter, summarises the features of AVC applied to series connected IGBTs. In addition, the author’s research contribution to series operation of IGBTs with the AVC technique, are stated and recommendations for future research are given.
CHAPTER ONE

Introduction

1.1 Power Electronics Advances in Medium to High Power Applications

Power electronics is incorporated into power areas where its benefits are cost effective. Early applications included power supplies and motor drives. Power electronics applications are expanding and new applications are emerging that lie between the areas of traction and industry and those of generation, transmission, and distribution (T&D). Table 1.1 lists a group of emerging applications that involve significant power electronics technology [1.1-1.19].

<table>
<thead>
<tr>
<th>Application</th>
<th>Description</th>
<th>Sector</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Active Filters</td>
<td>Compensates harmonic distortion in medium-voltage networks.</td>
<td>Power Quality</td>
</tr>
<tr>
<td>• Dynamic Voltage Restorer (DVRs)</td>
<td>Compensates drop in line voltage through external energy storage device.</td>
<td>Power Quality</td>
</tr>
<tr>
<td>• Static Compensator (STATCOM)</td>
<td>Correction of power factors, allowing voltage stabilisation and load balancing.</td>
<td>Traction, Industrial, T&amp;D</td>
</tr>
<tr>
<td>• Inter-ties</td>
<td>Ties asynchronous supplies together that are of identical or different phases.</td>
<td>Traction, Utility, Industrial</td>
</tr>
<tr>
<td>• Unified Power Flow Controller (UPFC)</td>
<td>Converter based system that allows control of power flow, voltage, and power factor.</td>
<td>T&amp;D</td>
</tr>
<tr>
<td>• Short DC Links</td>
<td>HVDC transmission links from utility to load and from alternate power source to grid.</td>
<td>T&amp;D</td>
</tr>
<tr>
<td>• Local Generation</td>
<td>Small turbo-generators running at high or variable speed requiring output frequency conversion.</td>
<td>Generation</td>
</tr>
<tr>
<td>• VARSpeed</td>
<td>AC excitation of synchronous motors-generators for speed control.</td>
<td>Generation</td>
</tr>
</tbody>
</table>
In the areas of traction and industry sectors, medium-voltage (2.3kV to 6.9kV) variable speed drives (VSD) are attracting the bulk of power electronics developments [1.20-1.22]. Early medium-voltage drive implementations suffered serious drawbacks, such as high harmonic content in input and output currents, poor power factor, and high common-mode voltage [1.20]. The drive systems required large floor area, had complex costly circuitry, and suffered high power losses. The major improvements in semiconductor switching devices, integrated circuitry, and microprocessors have significantly reduced the cost and decreased the power losses associated with medium-voltage drive systems.

In the areas of generation, transmission and distribution, the driving forces behind power electronics lay in the cost-effective implementation at the user level to either stabilise the voltages or to control the motor speed, acceleration, and torque [1.1]. In addition, Flexible AC Transmission System (FACTS) and High-Voltage DC (HVDC) transmission have engaged extensively with power electronics in several recent designs [1.19, 1.23]. The role of power electronics combined with power engineering enables efficient transmission and consumption of electricity, solving a large number of power transmission problems.

### 1.2 Power Semiconductor Devices

Power electronics systems have greatly benefited from advances in power semiconductor technology. The development of new devices and improvements in safe operating area have extended the use of self-commutating devices into high-power applications. Two main categories of self-commutated switching devices have been introduced in past decades and can be classified as shown in Table 1.2.

**Table 1.2: Available self-commutated semiconductor devices [1.1]**

<table>
<thead>
<tr>
<th>Thyristors</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>• GTO (Gate Turn-Off Thyristor)</td>
<td>• Bipolar Transistor</td>
</tr>
<tr>
<td>• MCT (MOS-Controlled Thyristor)</td>
<td>• Darlington Transistor</td>
</tr>
<tr>
<td>• MTO (MOS Turn-Off Thyristor)</td>
<td>• MOSFET</td>
</tr>
<tr>
<td>• FCTh (Field-Controlled Thyristor)</td>
<td>• FCT (Field Controlled Transistor)</td>
</tr>
<tr>
<td>• SITh (Static Induction Thyristor)</td>
<td>• SIT (Static Induction Transistor)</td>
</tr>
<tr>
<td>• IGCT (Integrated Gate-</td>
<td>• IGBT (Insulated Gate Bipolar</td>
</tr>
<tr>
<td>Commutated Thyristor)</td>
<td>Transistor)</td>
</tr>
</tbody>
</table>
Many of the emerging high power applications (greater than 1MW) will require the use of self-commutated switching devices [1.1], hence the selection of power semiconductor devices will eventually fall into the two main categories stated in Table 1.2. Though many device structures are reported, most remain restricted to low-power applications or remain in the realm of research [1.2]. Current devices set to dominate high power applications are the silicon-based IGCT [1.3] and IGBT [1.4]. The choice will depend on the circuit topology and system requirements, such as:

- Device and circuit costs;
- System reliability (low random failures, high power and temperature cycling);
- Efficiency for full and partial loads (low switching and conduction losses); and
- Structural size (few auxiliary components).

Figure 1.1 illustrates the present power range of commercially available IGCT and IGBT devices.

![Power range of commercially available IGCTs and IGBTs](image)

In medium-voltage or high-power applications, there are currently no power semiconductors available with sufficiently high-voltage capability to allow simple topologies. Series or parallel device connection becomes necessary. The main technology constraints faced by semiconductor manufacturers on producing higher voltage devices include [1.2, 1.12, 1.13]:

...
As voltage rating increases, so do switching losses and turn-off time, and they become significant in line frequency applications;

- The current density decays rapidly with increasing voltage in order for the device to stay within its Safe Operating Area (SOA), due to thermal considerations. This eventually decreases the output power rating; and
- Devices packaging and thermal management.

1.2.1. **IGCT – Integrated Gate-Commutated Thyristor**

Thyristor technology has superior performance characteristics to transistors when blocking voltages are above 2.5kV, as the on-state voltage loss is about half that of transistors, due to the greater charge density produced by the two emitters [1.5 pp. 272]. The IGCT (from ABB Industrial Systems) operates on the principle that it is an ideal conduction switch that makes no attempt to modulate transition speeds. It consists of an integrated gate driver that is device specific and hence simple to use, as the device switching speed cannot be altered to be faster or slower [1.3]. The switching transition is controlled by current signals at the gate electrode and the control power, which is typically of the order of 10 to 50W, depends heavily on the switched current and the pulse rate. Figure 1.2 shows the equivalent circuit for a power thyristor and the conducting and blocking state of an IGCT.

(a): Equivalent circuit of the thyristor (silicon controlled rectifier)

(b): IGCT conducting state

(c): IGCT blocking state

Figure 1.2: Characteristics of an IGCT
Although IGCT developments involve the technologies developed for the IGBT and recent GTOs [1.6, 1.15], it retains the thyristor latching nature and as such, cannot provide initial di/dt control. Instead, di/dt control is realised with a series passive choke in the circuit topology. In a typical IGCT inverter, as shown in figure 1.3, the DC link voltage is decoupled by a choke which controls the commutating diodes turn-off di/dt and the fault currents. The decoupling choke limits the fault current level in the event of failure of a bridge leg, since the IGCT is designed to behave as a short circuit when it fails.

![Figure 1.3: A typical IGCT inverter](image)

In medium and high voltage applications, the thyristor structure will be the favoured approach, especially where decoupling chokes are desirable or mandatory in the circuit topology. Currently available IGCT devices used in recent high-power applications include:

- A 20MW Metal Drive [1.7];
- A 25MW SMES (Superconducting Magnetic Energy Storage) [1.8];
- A 100MW BTB (Back-To-Back) Inter-tie using IGCTs [1.9]; and
- An 800MW BTB System using the GCT [1.10].

In practice, the design of high power applications using IGCTs needs to consider the following measures [1.11, 1.14].

- The IGCT produces a steep current transient (di/dt) at turn-on which can destroy auxiliary elements (commutating diode). Therefore, a turn-on protection circuit (di/dt snubber) is required in series with the device to limit the maximum rate of current rise;
The IGCT can only be connected in parallel when a second protection circuit (dv/dt snubber) is in parallel with the device. Alternatively, the turn-off timing has to be precisely synchronised on a nanosecond scale; and IGCTs connected in series will require a dv/dt snubber across each device in order to absorb the charge differences arising from device tolerances and temperature effects.

1.2.2. IGBT – Insulated Gate Bipolar Transistor

An IGBT is basically an integrated MOSFET and bipolar junction transistor structure. Essentially the IGBT is a MOSFET, plus a $p^+$ diffusion in the drain. It is a linear device where the switching transitions can be controlled by the gate drive. Through this controllability, the on and off transitions can be slowed down dramatically, making this switching device user-friendly. The required control power is low, typically in the order of 1 to 2W. Figure 1.4 shows the equivalent circuit and the cross-sectional view of a Punch-Through (PT) IGBT device.

![Equivalent circuit and cross-sectional view of IGBT](a) Equivalent circuit (b) Cross-sectional view of device structure

Figure 1.4: Overview of a PT-IGBT

IGBT flexibility and easy handling predestined it for a wide range of applications. Figure 1.5 shows a typical IGBT inverter. The advantage of the topology in figure 1.5 lies in the absence of auxiliary components, compared to IGCT inverter topology. However, at high voltages and powers, the absence of impedance between the power electronics (inverter) and the DC-link can result in high fault currents in the event of simultaneous failure of the devices in a bridge leg.
In medium or high voltage applications, series connection of IGBTs is necessary to overcome the present devices voltage limitation (6.5kV) and to provide a high redundancy system. With a redundancy design, the converter can continue operation even when one or two devices fail (short-circuit). Recent high-power applications utilising IGBTs include:

- 2MW medium-voltage converters [1.16];
- 2.4MVA medium-voltage drive [1.17]; and
- 50MW HVDC transmission system [1.18].

Like IGCT designs, utilising IGBT devices in high power designs has its own merits and limitations [1.1, 1.14]. They can be summarised as follows:

- No protective circuits, as required with the IGCT (di/dt snubber);
- The IGBT can be connected in parallel with few difficulties;
- The IGBT has a lower mobile charge carrier density during conduction compared to the IGCT, causing the IGBT conduction losses to be higher. However, the turn-off losses are lower as there are fewer minority carriers to be removed;
- The IGBT automatically, via the gate, limits the short-circuit current to between 5 and 10 times the rated current in the event of failure in external components (short-circuit in a motor winding or flashover) and the device can turn-off using the normal turn-off signal. The maximum SOA of the device causes no device damage if it is turned off within a 10μs period; and
Series IGBT connection is possible without using a turn-off dv/dt snubber if Active Voltage Control (AVC) is employed. Furthermore, the rate of rise to the off-state voltage in hard-switching IGBT applications is faster than with the IGCT. However, an appropriately insulated housing package is required for the IGBT, for redundancy reasons. A press-pack housing is favoured in series connection, as the semiconductor will form a reliable low-impedance path (short-circuit) in failure.

1.3 Silicon Carbide Power Devices

The potential for silicon carbide (SiC) semiconductor devices to replace silicon-based (Si) semiconductor devices in high-temperature and high-power applications has been discussed in the literature [1.29-1.35] for many years. The unique material properties of SiC allow better performance than Si devices for high-voltage applications because of its:

- High breakdown field;
- High saturated drift velocity; and
- High thermal conductivity.

These advantages allow a theoretical reduction in on-resistance by a factor of 100, and a maximum frequency 10 times higher than silicon [1.29-1.30]. In addition, the low reverse recovery current, even at high di/dt and high commutation voltages for SiC diodes, allows a drastic reduction of diode turn-off and turn-on losses with hard-switching [1.31-1.32]. However, the maximum operating temperature, particularly for the SiC Schottky diode, may be restricted due to increased leakage current [1.33]. Table 1.3 compares the basic material properties of silicon (Si) and silicon carbide (4H-SiC).

Table 1.3: Material properties of silicon and silicon carbide [1.29, 1.33]

<table>
<thead>
<tr>
<th>Property</th>
<th>Unit</th>
<th>Si</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap</td>
<td>eV</td>
<td>1.11</td>
<td>3.2</td>
</tr>
<tr>
<td>Breakdown Field</td>
<td>V/cm</td>
<td>6 x 10^5</td>
<td>35 x 10^5</td>
</tr>
<tr>
<td>(Layer doping, N_d = 1 * 10^17 cm^-3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Saturated Velocity</td>
<td>cm/s</td>
<td>1 x 10^7</td>
<td>2 x 10^7</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>W/cm/K</td>
<td>1.5</td>
<td>4.9</td>
</tr>
<tr>
<td>On-resistance</td>
<td>Ω</td>
<td>1</td>
<td>0.005</td>
</tr>
</tbody>
</table>
Although the data in Table 1.3 illustrates the superiority of SiC based switching devices, the defect density of SiC wafers is currently limiting commercially available high power devices [1.34]. The voltage and current ratings of SiC power devices will not exceed existing Si power devices until major improvements in SiC crystal growth enable larger defect-free areas [1.35-1.36]. Presently available SiC power devices include SiC diodes and SiC JFETs. Available diodes are limited to 600V and 12A [1.37]. The JFET device can be connected in series with a low voltage Si MOSFET in a cascaded topology as shown in figure 1.6, to achieve low on-resistance and overcome the normally-on characteristic of the SiC JFET [1.38]. This topology can be extended to several SiC JFETs connected in series for medium to high voltage applications. The current is currently limited to about 10A.

![Figure 1.6: Cascaded topology with high voltage blocking SiC JFETs in series with a low voltage Si MOSFET](image)

(a) Single JFET for lower blocking voltages
(b) Series connected JFETs for higher blocking voltages

SiC technology (like GaN and diamond) has gained wide attention as a future material for developing high-power switching devices. Unipolar SiC power devices may be practically utilised up to a 3.3kV blocking voltage if material quality and related costs are sufficiently developed. For higher blocking voltages, bipolar SiC power devices are more
suitable. However, significant progress in material quality, minority carriers lifetime, as well as lower production costs are required before SiC power devices are commercially viable for medium-voltage drives, transportation systems, and power distribution. Until these technologies and costs constraints are overcome, silicon-based power devices will dominate.

1.4 Summary
The advancement of power electronics technology has allowed great improvement and remarkable progress in the power capacity and switching speeds for medium-high power drives system. Power electronics has also penetrated into utility applications, such as HVAC and HVDC transmissions, allowing efficient system management.

The heart of power electronics technology lies in its semiconductor switching devices. Two particular switching devices dominate the present and possibly future high-power designs, the IGCT and the IGBT. Their high power ratings, high switching speed and simple gate drive control, allow them to excel in high-power applications. Although series connection is necessary, especially for IGBT designs, several recently commissioned high-power applications have proven their reliability and practicability. Ongoing research involves alternative device structures [1.24] and fabrication components [1.25] for the high-voltage IGBT. Figure 1.7 highlights power electronics technology advancement and the types of power semiconductor devices applicable to high-power designs.

Comparing the IGCT and the IGBT, the IGCT gate drive cannot control the rate of rise of current during turn-on. This requires a di/dt limiting inductor in the DC-link or in series with the device. In addition, the IGCT does not have an active, non-saturated region of operation. During fault conditions, the IGCT current is limited only by external circuit components, leading to rather complicated fault detection, protection, and shut down algorithms. However, present IGCTs are available in a medium-voltage, high-current press-pack device that can be used without recourse to series connection in medium power applications. Unlike the IGCT, the present available maximum IGBT voltage rating is 6.5kV in a module package [1.26, 1.27], making them unsuitable for series connection. Available press-pack IGBTs [1.28] of a lower voltage can be series connected for medium to high voltage designs. Table 1.4 compares the IGCT to the IGBT, for medium to high voltage applications.
Chapter One: Introduction

Power Electronics Technology

Early Applications
- Power Supplies
- Motor Drives

Emerging Applications
- Active Filters
- DVRs
- STATCOM
- Interties
- UPFC
- Short DC Links
- Local Generation
- VARSpeed

Chapter 1.1

Power Semiconductor Devices

Chapter 1.2

IGCT
- Available at MV Level

Chapter 1.2.1

IGBT
- Series connection required at MV Level

Chapter 1.2.2

Figure 1.7: The advancement of power electronics technology
<table>
<thead>
<tr>
<th>Comparison Parameter</th>
<th>IGCT</th>
<th>IGBT</th>
</tr>
</thead>
</table>
| • Control            | i) On/Off through current signals at the gate terminal.  
                        ii) No control during switching transients. | i) On/Off through voltage signals at the gate terminal.  
                        ii) Full controllability during switching transients. |
| • Parallel Connection| i) Require protection circuit (di/dt snubber). | i) Possible without protection circuit (active clamping, di/dt or dv/dt control). |
| • Series Connection  | i) Require protection circuit (dv/dt snubber). | i) Possible without protection circuit (active clamping, di/dt or dv/dt control). |
| • Short-circuit / Fault Protection | i) Device does not limit short-circuit current, thus a protective circuit is required.  
                        ii) Device short-circuits under failure conditions. | i) Device limits short-circuit current. Short-circuit may be shut off via normal gate signal.  
                        ii) Device is known to be short-circuiting only in press-pack housing during failure conditions. |
| • Power Losses       | i) Low on-state loss (symmetric charge distribution).  
                        ii) Low turn-on loss (di/dt snubber).  
                        iii) High turn-off loss (higher current density). | i) High on-state loss (larger wafer thickness and its charge distribution).  
                        ii) High turn-on loss (snubberless operation).  
                        iii) Low turn-off loss (lower current density). |
| • Gate Drive Circuit | i) High control power required.  
                        ii) Higher parts count but less sophisticated. | i) Low control power required.  
                        ii) Lower parts count but may be sophisticated. |
| • Reliability        | i) Proven in many commissioned high-power designs. | i) Not used extensively in high-power applications. |
| • Voltage Rating (6.5kV) | i) Available for most medium-voltage (MV) levels, at high current ratings. | i) Available for most medium-voltage (MV) levels but with lower current rating. |

Table 1.4: Comparisons of the IGCT and the IGBT, for medium to high voltage applications
References


[1.4] M. Rahimo et al., 'Extending the boundary limits of high voltage IGBTs and diodes to above 8 kV', Power Semiconductor Devices and ICs, 2002. Proceedings of the 14th International Symposium on, 4-7 June 2002, pp. 41-44.


Chapter One: Introduction


CHAPTER TWO

Literature Review of Inverter Methodologies

This chapter focuses on the different methodologies presented in the literature [2.1-2.27] for the development of medium-voltage (MV), high-power inverters. In order to overcome the limited voltage rating of semiconductor switching devices (6.5kV) in order to achieve the necessary medium-voltage levels, the topologies presented involve the switching devices being series connected, either directly or indirectly. This is shown in figure 2.1.

For MV inverters, several topologies [2.14-2.27] involve series connected power devices to produce a two-level output voltage. Simultaneous switching of the devices must be ensured and correct voltage sharing during switching and the off-state must be maintained to prevent device destruction. Multi-level inverter (MLI) topologies [2.1-2.13] produce smaller voltage steps to synthesis the output voltage waveform through asynchronous device switching.

These two main methodologies will be reviewed to illustrate their operating principle and merits and limitations.

2.1 Multi-level Inverters

Multi-level inverters (MLI) are made up from a family of inverter topologies [2.1-2.3], where the output voltage is developed from several intermediate voltage levels as shown in figure 2.2. Each intermediate voltage level is typically obtained from a capacitor voltage source. Commutation of the switches adds the capacitor voltages to the output voltage, which reaches a high voltage.

The three common multi-level circuit topologies that utilise capacitor voltages to synthesis their output voltage are:

- The Diode Clamped MLI;
- The Flying Capacitor MLI; and
- The Isolated H-bridge MLI.

Each topology has a specific switching algorithm for the series connected power devices in order to tap the capacitor high-voltage levels and refer these to the output [2.4]. The primary aim of all MLI circuits is to generate an output voltage which is much higher
than the voltage rating of the individual switching devices. An advantage of this methodology is reduced output harmonic content because of the small voltage step change in the output, which reduces the possibility of insulation breakdown in medium to high voltage drives.

Figure 2.1: Different methodologies for medium-voltage inverter legs using IGBT-based stack configurations
2.1.1 The Diode Clamped Inverter

The diode clamped inverter (DC-MLI) leg topology shown in figure 2.3 [2.5], is a widely used structure in multi-level inverters. It comprises series connected switching devices divided into sub-levels through the diode clamps which allow connection of each level capacitor to the output. An $n$-level diode clamped inverter typically consists of $n-1$ capacitors in the dc link and produces $n$ intermediate voltages levels. In the five-level MLI, the IGBTs connect the output to either the neutral point (midpoint of the capacitors, $n$), the positive dc link ($\frac{1}{4}V_{dc}, \frac{1}{2}V_{dc}$) or the negative dc link ($-\frac{1}{4}V_{dc}, -\frac{1}{2}V_{dc}$).
Table 2.1 indicates the relationship between the DC-MLI output voltage ($V_{an}$) and the IGBT switching states. There are five switch combinations to synthesize the five-level voltages of $V_{an}$. In the process of synthesizing the staircase voltage in each switching configuration, the voltage stress on each off-state IGBT is clamped to one capacitor voltage level. Hence the synthesized voltage levels produce an output waveform characterized by a lower harmonic content, compared to the two-level inverter output.

Table 2.1: Relationship between the five-level DC-MLI output voltage and the switch combinations [2.4]

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>Sw2ch2es</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>Diode Conducting Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{1}{2}V_{dc}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>D1</td>
</tr>
<tr>
<td>$\frac{1}{4}V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>$fb$</td>
<td>-</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>$fb$</td>
<td>-</td>
</tr>
<tr>
<td>$-\frac{1}{4}V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>$fb$</td>
<td>-</td>
</tr>
<tr>
<td>$-\frac{1}{2}V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$fb$</td>
<td>-</td>
</tr>
</tbody>
</table>

'0' indicates off, '1' indicates on, 'fb' indicates forward bias.

In Table 2.1, switches in the upper string, S1 to S4, are complementary to S1' to S4'. That is, for example, if S1 is on, then S1' is off and vice versa.

- For $V_{an} = \frac{1}{2}V_{dc}$, turn-on all the upper switches, S1 to S4. ($V_{an} = V_{C1} + V_{C2}$);
- For $V_{an} = \frac{1}{4}V_{dc}$, turn-on S2 to S4 and S1'. ($V_{an} = V_{C2}$);
- For $V_{an} = 0$, turn-on S3, S4 and S1', S2'. ($V_{an}$ is tied to the midpoint of the capacitors, $n$);
- For $V_{an} = -\frac{1}{4}V_{dc}$, turn-on S4 and S1' to S3'. ($V_{an} = V_{C3}$);
- For $V_{an} = -\frac{1}{2}V_{dc}$, turn-on all the lower switches, S1' to S4'. ($V_{an} = V_{C3} + V_{C4}$).
Ideally, the capacitors share equally the dc link voltage, provided no mean current is drawn from the neutral point. However, in practice, some form of control is needed to ensure capacitor charge balance [2.6]. Extending the number of voltage levels does not impose a higher voltage stress on an IGBT since it only blocks the voltage held by a capacitor, but some of the clamping diodes must have higher reverse blocking voltage ratings [2.4]. This diode feature is avoided by using the topology presented in [2.7].

The merits of utilising the diode-clamped, multi-level topology include:

- The control strategy is relatively simple, thus this MLI has received interest for industrial drives [2.8] and traction [2.9];
- Reactive power flow can be controlled as the capacitor voltages are balanced by equal charging and discharging during one operating cycle; and
- High efficiency, as all the switching devices are switched at the fundamental frequency (PWM operation is possible).

However, the limitations incurred include:

- Active balancing circuitry must be employed to ensure the capacitors remain equally charged in real power flow applications;
- Unequal device current ratings, as the switching devices have unequal duty cycles; and
- Theoretically the MLI is expandable to \( n \) levels [2.6] but the circuit becomes complex, both in terms of balancing the capacitors and the clamping diode requirements.

### 2.1.2 The Flying Capacitor Inverter

The flying capacitor MLI (FC-MLI) leg shown in figure 2.4, employs several capacitor banks precharged to different voltage levels. The capacitors for each bridge leg are independent and they are floating with respect to the earth. The capacitors, hence their voltage, are connected to the output using the series connected IGBTs. The synthesised voltage levels are similar to those of the DC-MLI. The storage capacitance requirements for the FC-MLI are equivalent to the \( n-1 \) capacitors for an \( n \)-level converter.
Table 2.2 indicates the relationship between the FC-MLI output voltage \( (V_{an}) \) and the various IGBT switching states. It is possible to create the required output voltage by series connection of the capacitors, thereby allowing current to flow in a direction required for capacitor recharging. The voltage synthesis states in a five-level FC-MLI offer more flexibility than the DC-MLI [2.4, 2.10] and each switching device need only switch once per carrier cycle. The switches \( S_1 \) to \( S_4 \) act complementary to switches \( S_1' \) to \( S_4' \), respectively.

Apart from the design issues related to balancing the capacitor voltages [2.11], the major problem with this topology is the large number of storage capacitors. When identical voltage rated capacitors are used for the FC-MLI, series connection of capacitors is required to achieve the necessary capacitor voltage requirements. This constitutes an increase of storage capacitors for each bridge leg. As with the DC-MLI, this topology also suffers from unequal device duty cycles.
Table 2.2: Relationship between the five-level FC-MLI output voltage and possible switch combinations [2.4]

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>Switches</th>
<th>Capacitor Charge Flow</th>
<th>Synthesised Capacitor Voltage Levels ($V_{an}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S1</td>
<td>S2</td>
<td>S3</td>
</tr>
<tr>
<td>$1/2V_{dc}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$1/4V_{dc}$</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
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<td>$0$</td>
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<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$-1/4V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$-1/2V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

'0' indicates off, '1' indicates on.

↑ indicates charge flow out of capacitor ⇒ +ve sign.

↓ indicates charge flow into capacitor ⇒ -ve sign.

The merits of utilising the FC-MLI include:
- The large storage capacitors allow ride through during power outages;
- Switch combination redundancy allows capacitor voltage balancing at most voltage levels; and
- Both real and reactive power flow can be controlled, making this topology suitable for HVDC transmission.
However, limitations include:

- Excessive number of storage capacitors are required as the voltage levels increase, making the overall structure bulky and expensive;
- Capacitor precharged circuitry is required and the control strategy becomes complex when the output is extended to three phases; and
- In real power transmission, inverter control becomes complicated and the switching losses associated with the switching frequency will be high.

### 2.1.3 The Isolated Cascaded H-bridge Inverter

The isolated cascaded H-bridge MLI (ICH-MLI) is considered the simplest MLI structure and is based on the series connection of single-phase H-bridges, each with a separate dc source [2.3, 2.12]. A chain of H-bridges (each can be considered a cell) is connected so as to generate the output pattern shown in figure 2.5. Each single-phase H-bridge is able to produce three output voltage levels, \(0, \pm V_{dc}\). The inverter output voltage waveform is synthesised by connecting the dc source of each single-phase H-bridge inverter sequentially to the ac side via its four switching devices.

Table 2.3 indicates the relationship between the ICH-MLI output voltage \(V_{an}\) and the IGBT switching states. The output voltage waveform is synthesised by the summation of the four H-bridge outputs. The requirement of an individual isolated dc voltage source for each H-bridge is the main limitation.

![Figure 2.5: A nine-level ICH-MLI leg [2.4]](image-url)
Table 2.3: Relationship between ICH-MLI output voltage and switch states for one H-bridge [2.4]

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$-V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

'0' indicates off, '1' indicates on.

- For $V_{an} = V_{C1} = V_{dc}$, turn-on S1 and S4. Each inverter output is sequentially added to build-up the output voltage to $4V_{dc}$.
- For $V_{an} = 0$, turn-off all switches. The isolated sources/capacitors are not involved.
- For $V_{an} = -V_{C1} = -V_{dc}$, turn-on S2 and S3. Each inverter output is sequentially added to build-up the output voltage to $-4V_{dc}$.

The merits of this multi-level topology include:

- It avoids high-voltage clamping diodes and storage capacitors;
- If more than five output voltage levels are required, this structure is deemed the most appropriate as the output voltage can easily be extended to $2n + 1$ levels, by series connection of $n$ H-bridges;
- It requires the least number of components among all topologies, for a given number of voltage levels;
- With equal conduction times of each switch in one operating cycle, the average capacitor charge change is zero. This allows capacitor voltage balancing to be achieved;
- The control strategy is simple, as each H-bridge is controlled independently;
- Modularised circuit layout and packaging is possible as each level has the same structure; and
- Possible elimination of the transformer when used in voltage dip compensation applications [2.13].
However, the limitations incurred include:

- Each individual floating cell requires an isolated dc source and
- Although both real and reactive power flow can be controlled, the requirement of separate dc sources limits this topology to applications involving back-to-back converters switched asynchronously [2.3].

2.2 Series Connected Power Devices

Unlike multi-level inverter topologies, series connected power devices in a MV inverter produce only a two-level output voltage and do not require steering diodes (except for free-wheel diodes) and have a common controller. A typical inverter structure is used and the number of series devices (or switch modules) is adjusted for the required blocking voltage, with the control electronics unchanged. Such an approach allows cost benefits from the future development of higher voltage devices and provides system redundancy, as the short-circuit failure of one or more devices need not halt operation.

Series connected power devices involves simultaneous switching of the series devices in order to achieve voltage sharing. Applications involving thyristor-based power devices (GTO thyristor, IGCT) are well-established [2.14-2.17], but require bulky passive circuit elements. Recent literature [2.18-2.27] has diverted to more controllable power devices (MOSFET, BJT, IGBT), in a search for less bulk and a more controllable system. Research has focussed on techniques to withstand a high blocking voltage and voltage balancing inspite of device parameter spread.

![Figure 2.6: A PWM-switched two-level output voltage from a MV inverter with series connected power device (one leg shown)](image-url)
Two direct series connected power device techniques are introduced, viz.:

- A hybrid series configuration and
- Series connected IGBTs.

### 2.2.1 Hybrid series configuration

The hybrid configuration or cascaded topology involves different types of power devices, series connected to achieve a higher voltage rating. Two hybrid configurations are reviewed to illustrate the basic operating principle, which circumvents present voltage rating limitations [2.18-2.19].

- Hybrid series connection of a controllable switch and thyristors and
- SiC cascaded power switches.

#### i) Hybrid series connection of a controllable switch and thyristors

Thyristors are suitable for high-voltage, high-power applications as they exhibit the highest voltage and power handling capabilities among Si switching devices and have a low on-state power loss characteristic. In this topology [2.18], a controllable power device (BJT, IGBT) is series connected with several thyristors (SCR, GTO), as shown in figure 2.17. The controllable turn-off capability of the bipolar device eliminates the auxiliary commutation circuits needed with thyristor-based devices.

![Figure 2.7: Hybrid series connection of a BJT and two thyristors](image-url)
In figure 2.7, the BJT is turned off by reversing its base current, causing the collector current to reduce, eventually reaching cutoff. As the thyristors are series connected with respect to the BJT collector, the anode current of each thyristor falls and once reaching the latching current, the thyristors turn off. During this process the collector current is diverted to the parallel connected snubber. This indirect control process allows the hybrid configuration to turn-off the thyristors without any auxiliary commutation circuits, whilst retaining the high blocking voltage characteristic of the thyristors.

The merits of utilising this topology include:

- Possible elimination of auxiliary commutation circuitry and
- Thyristor high-power handling capabilities can be utilised in medium-voltage, high-power applications.

However, the limitations incurred include:

- The anode current must remain below the latching current level for a certain time before the thyristors can block forward voltage. As such, the controllable switch will experience the forward voltage during this period. This voltage is reduced by the external RCD snubber;
- Individual device snubbers are required to achieve dynamic voltage balancing and this incurs extra losses, as well as limiting the switching frequency range due to the snubber set and reset action; and
- Well-matched controllable devices are needed as parameter spread results in different thyristor forward recovery times.

ii) **SiC cascaded power switches**

As with the hybrid configuration, the cascaded topology [2.19-2.20] utilises two different device structures to achieve a high-voltage rating. Figure 2.8 illustrates the series approach with a low-voltage Si MOSFET and several high-voltage SiC JFETs. The high-voltage SiC JFETs support most of the voltage during the blocking mode.
Figure 2.8: A cascaded circuit with a Si MOSFET and two SiC JFETs

The normally-on structure of the JFET is not suitable for voltage source inverter applications but with the series connected MOSFET, the series chain has a normally-off state. In general, the circuit behaves like a unipolar three-terminal device with the MOSFET gate accurately controlling the switching process. During the conduction mode, the MOSFET is turned on and this allows current to flow from the drain of J1 to the source of M1, as the on-state voltage of the low voltage MOSFET is insufficient to reverse bias the JFET into the off-state. The circuit transforms into a single MOSFET device with series resistive elements with current inhibiting ability. During the blocking mode, the MOSFET is turned off, and then the voltage bias starts to rise between the gate and source of J2 until the pinch-off voltage is reached. In a similar manner, the source of M1 together with the gate of J2 leads to channel pinch-off of J1. This feedback between the three devices enables the cascaded circuit to block high voltages.

The merits of utilising this topology include:

- As the JFET is able to conduct current in both directions, the MOSFET anti-parallel diode will act as the commutating device in inverter applications. Hence, the low voltage MOSFET has reduced storage charge in its anti-parallel diode during reverse recovery;
- The high-power handling capabilities of the SiC-based JFET can be employed in medium to high voltage applications; and
- A simple switching control strategy can be adopted, since the circuit can be viewed as a three-terminal MOSFET structure.
However, the limitations incurred include:

- Excessive power losses are generated due to the slow switching speed of the JFET and
- The slower switching speed of the JFET causes the MOSFET to avalanche during the blocking condition. Though MOSFETs are often designed for rugged avalanche behaviour, repetition in this switching mode should be treated with care.

### 2.2.2 Series connected IGBTs

Series connection of IGBT devices to form a chain of cells for blocking medium to high voltages has been demonstrated in the literature [2.21-2.27]. A modularised structure of series cells is possible as the control electronics is similar for all the devices.

The main design issues related to series connected IGBTs is the voltage sharing between devices during the static and transient states. In order to obtain the required high-voltage ratings, the voltage has to be distributed evenly among the devices. Two possible voltage control methods are introduced.

- Passive control and
- Active control.

#### i) Passive control

The passive control method normally utilises auxiliary passive elements, namely snubbers, to achieve dynamic voltage sharing [2.23]. Alternatively, auxiliary circuits composed of a transformer and commutating devices can be used to balance dynamic voltages [2.24]. Figure 2.9 shows the general structure for the passive control method when used with series connected IGBTs.

A simple resistive network, as shown in figure 2.10 with equal resistance, connected across each series device, can achieve static voltage balancing. With dynamic and static voltage sharing achieved, the structure is effectively a single IGBT that is capable of blocking high voltages.
The merits of utilising this series topology include:

- The snubbers reduce switching losses, resulting in a lower junction temperature, thus improving reliability and offering better thermal management;
- Lower EMI is produced due to reduced $dv/dt$ and $di/dt$ in the output; and
- Simple switching control strategy for the devices.

However, the limitations incurred include:

- The switching frequency range and duty cycle are limited due to the snubber set and reset times and
- Bulky passive elements and excessive power losses may occur in the auxiliary circuits.

\textbf{ii) Active control}

The active control method [2.25-2.27] relies on precise synchronised switching of the series connected IGBTs to balance dynamic voltages. Controlled gate drives eliminate snubbers and the structure can be viewed as a single IGBT device with precise controlled switching. Static voltage balancing is achieved with the resistive network shown in figure 2.10.
Figure 2.10: Series connection of IGBTs using active control

The approach merits are:
- Possible elimination of bulky passive circuit elements, resulting in a simple, cost effective structure and
- Manageable, controllable system with redundancy and fault detection.

However, the limitations include:
- Complex gate drive units;
- Elimination of passive snubbers has not been realised in practical applications, even with precisely controlled gate drives [2.27]; and
- Devices switching losses are increased.

2.3 Summary
The common objective of the considered methodologies, summarised in figure 2.11, is to enable present 'low' voltage power devices to be used in medium to high voltage applications. Each topology provides a method to circumvent device voltage limitations. The topology used for a particular application depends on the trade-off between system cost and circuit efficiency. The topologies involving series connected power devices are favoured over multi-level topologies in terms of circuit simplicity and redundancy. Such approaches are still in their infancy, especially for inverter applications.
Multi-level solutions have been demonstrated at the medium to high voltage level but several design factors need to be considered:

- An excessive number of steering diodes or storage capacitors are needed, particularly at high voltages;
- A large number of isolated dc sources are required for the high-voltage ICH-MLI topology;
- Multi-level designs need to utilise different control circuits at different voltages;
- Redundancy is not readily achievable with multi-level circuitry; and
- Capacitor voltage balancing is an issue.

Direct series connected IGBTs has been the focus of recent research and many medium-voltage drives are orientated towards this topology. The design issues that need to be considered for the medium-voltage inverter include:

- Dynamic voltage sharing needs to be ensured among the devices, accounting for device parameter spread;
- Static voltage sharing can be achieved with a simple resistive network, but results in high power resistors for high-voltage applications;
- The output voltage contains larger harmonic components than multi-level designs; and
- High output dv/dt stressing.
Figure 2.11: Overview of different methodologies and topologies for medium-voltage applications

References


CHAPTER THREE

Assessment of Series Connected IGBT Topologies

This chapter focuses on topologies involving series connected IGBT devices which attempt direct dynamic and static voltage sharing. Their operating principle and design considerations, with reference to medium-voltage drives, will be reviewed and assessed.

The topologies reviewed are grouped into two main control methods based on how switch dynamic voltage balancing is achieved, namely

- Passive control [3.1-3.4] and
- Active control [3.5-3.28].

The former methodology consists of passive elements or auxiliary control circuitry to ensure dynamic voltage sharing between the devices. Whereas the latter methodology is dependent on gate drive linear control techniques to circumvent the spread of IGBT switching parameters. The various techniques are pictorially classified in figure 3.1.

![Diagram](image)

Figure 3.1: Two main methodologies for series connected IGBTs
Series connected IGBT research has focused on developing techniques for achieving voltage sharing of each series device during transient and off-state conditions. Unbalance voltage sharing during the transient-state results in the device that recovers first from turn-off or last from turn-on, possibly experiencing the full-supply voltage. If the parameter spread in terms of device leakage current is significant, the device that has the largest leakage resistance (lowest leakage current) during the steady-state will support a higher blocking voltage. Either of these mechanisms, shown in figure 3.2, can cause catastrophic device failure [3.11]. Static voltage balancing in most of the literature is achieved with a simple resistive network structure as shown in figure 3.3, while dynamic voltage sharing is the primary research concern.

![Figure 3.2: Unequal voltage sharing during dynamic and static conditions](image)

### 3.1 Off-state and turn-off voltage sharing

#### 3.1.1 Static voltage sharing - traditional theory

The equalising resistors $R_s$ in figure 3.3a are necessary to ensure equal division of the supply voltage $V_s$ among the series IGBTs during the off-state. Calculation of the required static voltage sharing resistance $R_s$ [3.29, pp. 220] is based on the spread of device off-state leakage current, $\Delta I_L$, at a given voltage and temperature, under worst case conditions:

$$R_s = \frac{nV_D - V_s}{(n-1)\Delta I_L} \quad (\Omega) \quad (3.1)$$

where $n \geq 2$ is the number of devices.
\[ \Delta I_L = I_{b(\text{max})} - I_{b(\text{min})} \] (A)

\[ = I_1 - I_2 \] (A)

While the maximum total power, distributed between the \( n \) resistors, is given by:

\[ P_R = \frac{V_s^2}{nR_s} \] (W) (3.2)

### 3.1.2 Dynamic voltage sharing - traditional theory

During turn-off, the differences in junction capacitance and recovery charges among the series IGBTs causes differences in blocking voltage sharing and it is normally necessary to connect a capacitor, \( C_s \), across each devices as shown in figure 3.3b. The capacitor function is to dominate the collector voltage rise rate at turn-off which allows balanced voltage sharing due to the turn-off transient, diode reverse recovery and IGBT tail current differences. Calculation of the required dynamic voltage sharing capacitance, \( C_s \), is based on the difference in the stored charge of the IGBTs and can be specified by [3.29, pp. 224]:

\[ C_s = \frac{(n - 1)\Delta Q}{nV_D - V_s} \] (F) (3.3)

where

\[ \Delta Q = Q_{\text{max}} - Q_{\text{min}} \] (C)

**Figure 3.3:** Equal value of \( R_s \) and \( C_s \) across each switching device for

(a) static and (b) dynamic voltage balancing
While a resistive network is electrically effective and cost effective for static voltage balancing, the use of a capacitance network for transient voltage sharing is not favoured. This is because in worst case design, the capacitance may be extremely high and the capacitance energy is dissipated in the switch at turn-on. Matched devices minimises requirements. Possible alternatives are now considered.

3.2 Passive Control utilising Passive Elements

This approach depends on snubber circuits to achieve turn-off dynamic voltage balancing. The technique has been used in many practical medium to high voltage applications which use series connected IGCTs or IGBTs [3.4]. The control techniques for turn-on dynamic sharing have received little attention, since parameter spread between devices is more significant during the turn-off transient, due to the Miller capacitance effect.

3.2.1 J.F. Chen et al.

The technique demonstrated by the authors [3.1] is based on the conventional RCD snubber used in many design applications for reducing switch turn-off voltage stress.

As shown in figure 3.4, each device has an RCD snubber for turn-off dynamic voltage balancing and a balancing resistor for static voltage sharing. The capacitor (via the diode) in the snubber circuit limits the rate of rise of collector voltage across each device during the turn-off transient. With large capacitance and small parameter tolerances, the collector...
voltage rate of rise will be dominated by the snubber circuit. Any overshoot voltage can be constrained to a safe level. This conventional technique is the easiest way to obtain turn-off dynamic voltage balancing.

The advantages of this topology for medium-voltage drives include:

- Simple structure with minimal component count and simple gate drive circuit;
- Well-proven circuit reliability in many medium to high voltage applications [3.4]; and
- Turn-off losses in the switching devices are significantly reduced.

However, the disadvantages incurred include:

- The snubber passive elements have a high voltage rating, making them bulky and costly;
- Matched capacitance is required to ensure the same voltage rise rate for all the devices;
- High power loss due to dissipation of snubber capacitor energy but this is in a resistor that may be remotely located; and
- Minimum IGBT on-time is determined by the snubber discharge time.

3.3 Passive Control utilising Auxiliary Circuitry

Two topologies that are classified under this methodology, demonstrate that turn-off dynamic voltage sharing can be achieved through passive auxiliary circuitry. Both circuits use a capacitor across each device to limit the rate of rise of the collector voltage across each device.

3.3.1 G. Busatto et al.

The technique shown in figure 3.5 is based on an auxiliary coupled circuit connected between two series-connected IGBTs which create a flyback-converter, therein ensuring uniform distribution of the voltage on the series devices [3.2].

The capacitors store the excess voltage energy of the faster device during turn-off and this energy is transferred to the primary side of an isolated transformer (L1 or L2). Some of this energy is simultaneously dissipated in $R_d$ on the secondary side of the transformer.
Dynamic voltage sharing is assured by the snubber capacitor in parallel with each device. The snubber capacitance can be small due to the clamping function.

![Figure 3.5: Schematic diagram of the passive auxiliary control circuit](image)

The advantages of this topology include:

- Hard-switching is possible if the snubber capacitance is small and
- No sophisticated gate drive technique is needed.

However, the disadvantages include:

- This approach results in great complexity when the number of series devices is increased and
- The steady-state on-time has to be sufficient for the snubber capacitor to fully discharge before the next off transition. This will limit the switching duty-cycle, especially when using PWM switched topologies.

### 3.3.2 J.W. Baek et al.

The technique shown in figure 3.6 is based on an auxiliary circuit acting on the gate of the switching device to ensure voltage balancing among the series devices [3.3].

The auxiliary circuit uses six passive components to achieve both static and dynamic voltage balancing. The control approach can be described with reference to the charging of capacitor C2 during an overshoot voltage condition. Over charging of C2, through C1 causes the IGBT to turn on thereby absorbing the overshoot voltage energy. The divider resistors facilitate static balancing and dynamic balancing is obtained by the divider capacitors. The auxiliary circuit diode decouples the auxiliary circuit from the gate terminal during steady-state operation.
Chapter Three: Assessment of Series Connected IGBT Topologies

Figure 3.6: Schematic diagram illustrating the auxiliary control circuit

The advantages of this topology include:

- Minimum component count and simple structure and
- The circuitry can be extended to multiple series-connected IGBTs without escalating complexity.

However, the main disadvantage is that:

- The voltage across the upper capacitor C1 has to be maintained at a constant level regardless of the switching transients, resulting in a large capacitance requirement.

### 3.4 Active Control with Snubber Circuits

Synchronous switching or precise gate current control to achieve dynamic voltage balancing is the basis of the active control method. Although the technique eliminates snubbers from the circuit, the three topologies reviewed need a small RC snubber. The capacitance is much smaller than in the conventional snubber circuit used in the passive control method. As such, active gate drive techniques focus on parameter spread compensation via individual gate drive circuits and utilise the RC snubber to minimise the effect of IGBT and anti-parallel diode non-linear junction capacitances. Static voltage balancing is ensured by a resistive network across each series devices.
3.4.1 J. Sigg et al.

The active gate drive technique in figure 3.7 involves overshoot voltage detection which acts on the IGBT gate to secure symmetrical voltage sharing [3.5-3.6]. The overshoot-voltage circuit is in the feedback path between the IGBT collector and its gate, and detects and provides control of the maximum collector voltage experienced by the switching device.

![Schematic diagram of the over-voltage control circuit](image)

Figure 3.7: Schematic diagram of the over-voltage control circuit

At the gate level, the output from the overshoot voltage circuit is compared with the reference voltage from the control circuit. The resultant difference voltage is amplified and used to control the IGBT transient-states. In the situation where one series device turns off earlier than the others, the collector voltage rises only to the maximum voltage level specified by the protection circuit. The collector voltage is maintained at the maximum level by controlling the IGBT in the active region until the other switching devices turn-off.

The advantages of this topology include:

- The control circuitry can be extended to multiple series devices without escalating complexity and
- It provides dynamic voltage control for both turn-off and turn-on.
However, the disadvantages include:

- The fastest switching device may experience excessive switching losses due to the requirement for that device to remain in the active region during the clamping process and
- A response delay occurs before the protection control circuit actively clamps the IGBT, increasing the overshoot voltage of the clamped IGBT.

### 3.4.2 S. Hong et al.

The active gate drive circuit in figure 3.8 consists of analogue circuitry to limit the overshoot-voltage seen by the series devices during dynamic unbalanced switching conditions [3.7-3.8].

![Figure 3.8: The active voltage balancing control scheme](image)

Active gate control functions only when the IGBT voltage exceeded a pre-determined voltage level. The detection circuit comprises a simple resistive divider network across the device to feedback the scaled-down collector voltage which is compare with a pre-determined reference. When the feedback voltage exceeds the pre-determined level, the excess voltage is converted into positive gate current, which is constantly applied to the gate until the feedback voltage falls to a level lower than the pre-determined voltage. Effectively gate to emitter capacitance discharge is slowed by the applied positive gate current. During turn-on, the positive gate current enhances gate to emitter capacitance...
charging. This allows the slower switching device to respond and support overshoot voltage.

The advantages include:

- The active gate drive circuit can be extended to multiple series devices without escalating complexity;
- The active controller does not operate or create any delay or power loss in the IGBT when the overshoot voltage is less than the excess voltage region; and
- The active controller includes dynamic voltage control for both turn-off and turn-on conditions.

However, the disadvantages incurred include:

- Excessive switching losses result, as the device is prolonged in the active region during the control process and
- The active elements in the control circuitry are maintained in the active region to ensure fast response to any overshoot voltage. This leads to power losses in the control circuitry and heat dissipation is a concern in high-temperature environments.

3.4.3 **B.S. Seo et al.**

The technique shown in figure 3.9 attains voltage balancing by actively controlling an RCD snubber circuit across each device. Active control minimises the snubber capacitance [3.9-3.10].

The snubber capacitance is initially connected to the IGBT gate. The Miller capacitance during the turn-off stage is effectively large which slows the voltage rise of the switching device. This allows slower devices to respond, before a second stage is initiated. This subsequent stage connects the snubber capacitance across the IGBT collector to emitter in order to allow the collector voltage to rise quickly. The turn-off time for all the devices is synchronised by the control algorithm incorporated in the control circuitry.
Figure 3.9: Schematic diagram of the control circuit in the RCD snubber circuit

The advantages of this topology in medium-voltage drives include:

- The control circuitry can be extended to multiple series devices without escalating complexity and
- Smaller snubber capacitance can be used to reduce power losses and equipment size.

However, disadvantages incurred include:

- Although snubber capacitance is reduced, the control process can result in increased switching losses and snubber reset may limit the switching frequency range and
- Matched snubber capacitance and a fast response control circuit are required to ensure synchronised turn-off of all the devices.

3.5 Active Control without a Snubber Circuit

Unlike active control methods that utilise a snubber circuit to compensate the device, the eight topologies reviewed now are based solely on an active gate drive to achieve dynamic voltage balancing, regardless of device or gate drive parameters spread. Static voltage balancing in general depends on a resistive network across each device, however
alternative methods include a static balancing controller [3.11] and an active clamping circuit [3.22].

### 3.5.1 C. Gerster et al.

The active gate drive unit driving the series-connected IGBTs shown in figure 3.10, is controlled by a digital signal processor (DSP) [3.11-3.12]. The control algorithm for dynamic and static voltage balancing, adjusts the time delay for each gate signal.

Dynamic voltage balancing is achieved by delaying the turn-off and turn-on edges of each IGBT gate signal in a controlled manner. The transient and static voltage balancing controllers are implemented as dead-beat-controllers [3.13] in the DSP which functions as a time-discrete digital controller synchronised to the switching signal. By sensing the feedback voltage across the device, the controller produces the required signal delay for each gate signal.

The advantages of this topology include:

- Fast switching speed is possible without increasing the total switching losses and
The control methods for dynamic and static balancing can be integrated into a single intelligent gate drive.

However, the disadvantages incurred include:

- The control topology is dependent on the accumulation of sample data which may limit performance effectiveness in drastic operating conditions that involved sudden terminal voltage variations or at start-up and
- Although the active gate drive can be extended to multiple series devices, the control circuitry may result in great complexity to ensure precise device switching control.

3.5.2 S. Musumeci et al.

The active gate-controlled technique shown in figure 3.11 is based on a master and slave concept where the first switching device in the series chain is considered the master and the remaining devices are slaved [3.14-3.17]. The master switch is hard driven. Active gate drive is applied to the slaved devices and the collector voltage of the master device is feedback to the active gate drive as the reference voltage signal.

![Figure 3.11: Schematic diagram illustrating the Master-Slave approach](image)

Dynamic voltage control by the active gate drive is through controlling the device switching times with gate current injection during the Miller effect period. The drive
strategy is based upon independent control of the dynamic voltage across each device by controlling and synchronising the gate current according to detection feedback of the Miller zone. The active gate drive has a conventional push-pull output stage, and a current generator and current sink. The function of these current units is to inject or extract precise current into or out of the parasitic capacitance of the controlled switching device. The current source is selected depending on the comparison between the master device reference voltage and the slave device collector voltage.

Circuit advantages include:

- Hard-switching is possible and
- The active gate drive includes dynamic control for both turn-off and turn-on.

However, the disadvantages incurred include:

- The sensing network for the feedback voltage to each active gate drive becomes complicated as the number of series devices increases and
- The functionality of the master switching device is critical to the operation of the slave devices. Failure of the master device will result in loss of dynamic voltage balancing control.

3.5.3 K. Sasagawa et al.

The active gate drive technique in figure 3.12 utilises magnetically coupled transformers in the gates of the series-connected IGBTs [3.18].

Figure 3.12: Schematic diagram illustrating the Gate-Balancing-Core transformer method
The transformer windings are wound unpolarised so as to produce a compensating gate current. In the event of a gate timing imbalance, the gate signals difference creates a voltage pulse on the gate drive, that either assists or resists the charging or discharging of the gate capacitance during transient states. This results in identical gate current signals for all the series devices.

The advantages of this topology include:

- Fast switching is possible and
- The active gate drive circuit includes dynamic voltage control for both turn-off and turn-on.

However, the disadvantages incurred include:

- The transformer core must not saturated and this may limit the duty-cycle, especially in PWM switched topologies;
- Dynamic voltage balancing is based on two devices being magnetically coupled. This may prevent redundancy when one device fails;
- High gate current (in the range of 9A) is required for a fast response to compensate imbalanced gate timings. This leads to a large power source for the active gate drive circuit; and
- This method only compensates gate drive timing errors.

3.5.4 **D. Zhou et al.**

The control technique shown in figure 3.13 attains voltage balancing through the combination of device voltage clamping and gate signal delay compensation [3.19].

The voltage clamping circuit limits the overshoot voltage during start-up or extreme operation, while the signal delay control circuitry produces dynamic voltage balancing. The device terminal voltage is compared with a pre-determined threshold and the result is used to adjust the gate signal so as to clamp the overshoot. The gate signal is adjusted by analogue delay circuitry. The combination of both analogue and digital control provide precise delay for compensating different IGBT response times. The clamping circuit uses series connected high-voltage Zener diodes (Transorbs) between the IGBT collector and gate.
The advantages of this topology for use in medium-voltage drives include:

- Hard-switching is possible and
- The clamping circuit is capable of limiting an overshoot voltage sustained during both turn-off and turn-on.

However, the disadvantages incurred by this topology include:

- The system may require several cycles to compensate for the different delay times. During this period, clamped devices will experience high switching losses;
- Excessive component count, especially the number of Zener diodes to attain high voltages; and
- The synchronisation of the delay signals may be affected at high temperature.

3.5.5 H. Nakatake et al.

The control technique shown in figure 3.14 involves two gate circuit functions to clamp the overshoot voltage during turn-off and the tail current period [3.20].

The gate control circuit includes a multi-level clamp circuit and a turn-off timing adjustment circuit. The multi-level clamp circuit reduces the collector voltage rise rate in order for the clamping circuit to respond to overshoot voltage conditions. This stops the device from sustaining a high overshoot voltage, preventing additional power losses. The
turn-off timing adjustment circuit controls or adjusts the turn-off gate signal according to the imbalance voltage detected during the tail current period.

![Block diagram illustrating two gate control circuits](image)

**Figure 3.14: Block diagram illustrating two gate control circuits**

Advantages include:
- The active gate drive circuit minimises the overshoot voltage sustained by the device and
- The imbalance voltage sharing during the transient state and tail current period is actively clamped.

However, the disadvantages incurred by this topology include:
- Although the peak overshoot voltage is minimised, the device still incurs additional switching losses due to the reduced collector voltage turn-off rate and
- A large number of components are required.

### 3.5.6 S. Katoh et al.

The active gate-controlled circuit shown in figure 3.15 is based on active clamping of the collector voltage during imbalanced dynamic conditions [3.21].

The gate drive consists of four main functional blocks and their functions include producing the required gate voltage reference signal for IGBT switching and collector voltage clamping. Within the control circuitry, two current sources charge or discharge the gate capacitance, depending on the differential error voltage produced. When the
collector voltage exceeds the specified blocking voltage during turn-off, the IGBT is turned on to actively clamped the overshoot voltage, until it falls below a specified level.

![Schematic diagram illustrating the gate drive unit control blocks](image)

Figure 3.15: Schematic diagram illustrating the gate drive unit control blocks

The advantages include:

- Hard-switching is possible and
- Both dynamic voltage control of turn-off and turn-on are incorporated.

However, the disadvantages incurred by this topology include:

- Excessive switching loss is sustained during the active clamping period and the device has to be rated to support the overshoot voltage and
- A fast response time is necessary for the gate drive.

3.5.7 A. Piazzesi et al.

Balanced voltage sharing among the series devices is produced by the circuit in figure 3.16, with an active clamping circuit that ensures both dynamic and static voltage control [3.22-3.23]. The collector voltage is actively clamped when it exceeds specified voltage levels, giving both dynamic and static balancing.
The active clamping circuit has several series-connected Zener diodes (Transorbs) between the IGBT collector and gate. Two threshold voltages are implemented for dynamic and static balancing. During an overshoot voltage at turn-off that exceeds the dynamic threshold voltage level, the Zener diodes (Dz1 and Dz2) clamp the excessive collector voltage by feeding back current into the gate. This results in turn-on of the switching device to reduce the collector voltage. In addition, a 'Miller' capacitor (C1) is added across one Zener diode to reduce the collector voltage rise rate. The static threshold voltage level is much lower and the Zener diode (Dz1) clamps any excessive voltage during the off state.

![Clamping Circuit Diagram](image)

**Figure 3.16**: Schematic diagram illustrating the active clamping circuit

The topology advantages include:

- Hard-switching is possible and
- The active gate drive incorporates control for both static and dynamic conditions, eliminating any passive components across the devices for static balancing.

However, topology disadvantages include:

- Excessive power losses have to be dissipated by the Zener diodes, especially at high voltages and
Although active clamping is operated only when the collector voltage exceeds threshold levels, failure of one device will impose an additional blocking voltage across the remaining functional units. This extra voltage may exceed the original specified threshold levels and result in constant clamping of the collector voltage.

3.5.8 P.R. Palmer et al.

The active gate-controlled technique shown in figure 3.17 is based on forcing the IGBT collector voltage to follow a reference input signal [3.24-3.28].

Figure 3.17: Schematic diagram illustrating the active voltage control technique

The circuit consists of a differential amplifier that compares the collector voltage feedback from the resistor sensing network with a specified reference signal. The differential output voltage feeds the IGBT gate. In order for the IGBT to track the reference signal, a pre-conditioning step is imposed on the reference signal to overcome the gate delay and non-linear gate capacitance. This pre-conditioning step is implemented only at the turn-off transition, as the Miller capacitance is more significant than at turn-on. The sensing network for feedback detection is a resistive divider circuit.
The advantages include:

- High peak overshoot voltages can be eliminated and
- Full control of the collector voltage makes this technique appropriate to redundancy designs.

However, the disadvantages incurred include:

- Control of the collector voltage transition rate is gained at the expense of higher switching losses and
- If fast response of the gate drive is required, this technique may not be appropriate.

3.6 Summary

The different static and dynamic voltage balancing topologies proposed in recent publications have been categorised into two main groups, as shown in figure 3.18, namely

- Load side control and
- Gate side control.

Load side control involves topologies with passive control that utilises passive elements or auxiliary circuits to achieve voltage sharing among series connected devices. Gate side control involves topologies with active control that modifies the gate drive signal to ensure voltage sharing. The main limitations of load side control are the bulky and costly passive components that induce additional system losses. However, the reliability of this method has been well-proven in many medium to high voltage applications. Although gate side control topologies allow the possible elimination of the passive components acting to reduce the collector voltage rate of change, the complexity of the gate drive and redundancy design issues limit this method in medium to high voltage applications. A small RC snubber is needed across each switching device in active gate drive applications. Table 3.1 indicates the control circuitry involved for each topology and their advantages and disadvantages in medium-voltage drive applications.
## Chapter Three: Assessment of Series Connected IGBT Topologies

<table>
<thead>
<tr>
<th>Description</th>
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Note: ![ ] indicates 'yes' in the category stated.

Table 3.1: Comparison of control topology in achieving dynamic voltage balancing
Figure 3.18: Categorising the different topologies into Load Side Control and Gate Side Control for series connected IGBTs

References


Chapter Three: Assessment of Series Connected IGBT Topologies


CHAPTER FOUR

Overview of IGBT Gate Drive Aspects

Series operation of IGBTs through active voltage control requires device gate signals to be accurately controlled during the switching transitions. Apart from incorporating a dynamic voltage balancing method, gate drive performance and efficiency must be considered. This chapter considers recently published IGBT gate drive topologies and focuses on their design features which reflect on IGBT switching losses and fault protection.

Figure 4.1: Main design factors of an active gate drive circuit

4.1 IGBT Switching Behaviour

The switching behaviour of the MOSFET is applicable to the IGBT. Both devices have similar switching characteristics during turn-on but differ during the latter part of the turn-off process. The IGBT has a current tail during the decay of its collector current. This current tail is due to recombination of the excess minority carrier charge in the IGBT drift region. The tail charge is unaffected by the external circuit [4.1, pp. 476-479]. The ideal switching characteristics of an IGBT are shown in figure 4.2, for a step gate input voltage source [4.2, pp. 86-88].
4.1.1 Turn-on

The turn-on process is divided into the four phases shown in figure 4.2a. Phase one corresponds to the IGBT turn-on delay time, $t_{d(on)}$, due to the charging of the input capacitance, $C_{in}$. The duration of this delay time is dependent on the gate resistance, $R_g$, and the magnitude of the input voltage source, $V_g$.

$$t_{d(on)} = R_g C_{in} \ln \left( \frac{V_g}{V_g - V_{ge(th)}} \right)$$  \hspace{1cm} (4.1)

where $V_{ge(th)}$ is the turn-on threshold gate voltage.
Phase two commences once $V_{ge(\text{th})}$ is reached and the collector current $I_c$ rises. The gate-emitter voltage, $V_{ge}$, continues to rise during this period. The collector current risetime, $t_r$, is determined by:

$$
t_r = R_g C_m \ln \left( \frac{V_g}{V_g - \left( V_{ge(\text{th})} + \frac{I_s}{g_m} \right)} \right) (s) \tag{4.2}
$$

where $I_s$ = conducting current (A)

$g_m$ = transconductance (S)

Phase three occurs when $I_c$ reaches the maximum value $I_s$ and the Miller effect is observed in $V_{ge}$ as the gate-collector capacitance, $C_{gc}$, is charged by the constant gate current, $I_g$ [4.3]. $V_{ge}$ is constant at $V_{ge(\text{th})} + \frac{I_s}{g_m}$ as the collector-emitter voltage, $V_{ce}$, begins to fall. The initial steep voltage fall during $t_fv(1)$ is due to the small $C_{gc}$ at turn-off. $C_{gc}$ increases as the switching transition moves toward turn-on, resulting a slower voltage fall during $t_fv(2)$. Assuming a negligible on-state voltage drop, the total collector voltage falltime is a function of $I_s$, $I_g$, $C_{gc}$, and output capacitance $C_o$, and is given by:

$$
t_{fv} = V_s f \left[ I_s, I_g, C_{gc}, C_o \right] (s) \tag{4.3}
$$

In the plateau region, the rate of change of collector voltage, $dV_{ce}/dt$, is given by:

$$
\frac{dV_{ce}}{dt} = \frac{1}{C_{gc}} \frac{V_g - V_{ge}}{R_g} (V/s) \tag{4.4}
$$

On reaching phase four, $V_{cc}$ has decayed to the on-state voltage level and the gate voltage rises to the input source voltage, $V_g$.

### 4.1.2 Turn-off

The turn-off process is divided into three phases, as shown in figure 4.2b. Phase five is the turn-off delay time, $t_{d\text{off}}$, when the gate input source voltage drops to zero. The delay time is due to discharging of the input capacitance and is given by:

$$
t_{d\text{off}} = R_g C_m \ln \left( \frac{V_g}{V_{ge(\text{th})} + \frac{I_s}{g_m}} \right) (s) \tag{4.5}
$$
Once the gate voltage reaches \( V_{ge(th)} + \frac{1}{g_m} \), phase six commences and \( V_{ge} \) remains constant as the IGBT builds up its forward blocking voltage. The variations of \( C_{ge} \) during the turn-off transition results in two periods \( t_{rv(1)} \) and \( t_{rv(2)} \). The slow change during \( t_{rv(1)} \) is due to a large \( C_{gc} \) and the faster change during \( t_{rv(2)} \) is due to the decrease in \( C_{ge} \). The total collector voltage risetime is a function of \( I_s, I_g, C_{ge}, \) and output capacitance \( C_o \), and is given by:

\[
\tau_v = V_s f \left[ I_s, I_g, C_{ge}, C_o \right] \quad (s) \quad (4.6)
\]

In the plateau region, the rate of change of collector voltage, \( \frac{dV_{ce}}{dt} \), is given by:

\[
\frac{dV_{ce}}{dt} = \frac{1}{C_{gc}} \left[ \frac{V_g - V_{ge}}{R_g} \right] \quad (V/s) \quad (4.7)
\]

The collector current falls in phase seven when the IGBT supports the blocking voltage, \( V_s \). The current decay is divided into two parts. The initial rapid fall is due to the termination of the electron current in the inherent MOSFET structure, as a result of the disappearance of its conducting channel inversion layer. Although the MOSFET is turned off, the excess minority carriers stored in the drift region during the on-state provide the continued flow of hole current in the BJT section. This leads to the tail current seen in the latter part of phase seven. The current fall-time in the first part of stage seven, due to the MOSFET action, covers the period from the start of the \( I_c \) fall to the turn-off threshold voltage level and is given by:

\[
t_{fi(1)} = R_g C_{in} \ln \left( 1 + \frac{I_s}{g_m V_{ge(th)}} \right) \quad (s) \quad (4.8)
\]

After this, the collector current decays at a rate determined by the carrier lifetimes of the PNP transistor charges. To derive an expression for this period, the current is assumed to decay in a high-level injection condition within the n-drift region and the carrier lifetime remains independent of the injection level \([4.1, pp. 478]\).

\[
t_{fi(2)} = \tau_{HL} \ln(\alpha_{pnp}) \quad (s) \quad (4.9)
\]

where \( \tau_{HL} \) = high-level carrier lifetime \( (s) \)
\( \alpha_{pnp} \) = current gain of the PNP transistor

The IGBT collector current fall-time, \( t_{fi} \), is therefore given by:

\[
t_{fi} = t_{fi(1)} + t_{fi(2)}
\]
\[ \tau_{HL} \ln(\alpha_{npp}) \]  

\[ \text{(4.10)} \]

4.2 IGBT Gate Drive Topologies

The efficiency and reliability of the IGBT as a superior switching device is strongly influenced by its gate drive circuit. Recent literature [4.4-4.20] on IGBT gate drive topologies focuses on improving the switching performance and includes additional control features for short-circuit protection and to reduce collector voltage stresses. The review of the gate drive techniques in this chapter is divided into two parts:

- Enhancing IGBT switching performance [4.4-4.11] and
- IGBT fault protection [4.12-4.20].

4.3 Enhancing IGBT Switching Performance

The conventional IGBT gate drive circuit is based on pure resistive gate control as shown in figure 4.3. The gate voltages 0V and \( V_g \), are switched to the IGBT gate by the polarised gate resistances, \( R_{g(off)} \) and \( R_{g(on)} \), and the switching speed can be controlled by these resistors. The drawback of pure resistive control is that the collector switching current and voltage cannot be separately controlled to reduce the switching losses and stresses. The switching losses increase with higher gate resistance and any variation of the polarised gate resistances will affect the switching and delay times. The conventional gate drive is unable to independently control \( dV_{ce}/dt \), \( dI_L/dt \), overshoot voltage at turn-off, and peak turn-on current due to the reverse recovery of a free-wheel diode, without increasing the switching losses. Seven active gates drive topologies [4.4-4.11] are considered, which overcome the drawbacks of pure resistive gate control and attempt to optimise IGBT switching performance.

![Figure 4.3: Conventional gate driver with pure resistive control](image-url)
4.3.1 B. Weis et al.

The gate drive circuit in figure 4.4 illustrates the control technique used to vary the gate resistance during turn-off in order to suppress a collector voltage surge [4.4]. During the initial turn-off process, transistors Q1 and Q2 are on in order to achieve a low gate resistance for rapid discharge of the input capacitance. Once the collector voltage exceeds the breakdown voltage of the Zener diode Dz1, the dVce/dt detection circuit produces a current pulse to the triggering circuit. The monostable output switches Q1 off for an interval. This increases the collector current fall-time since the discharge of the input capacitance is now determined by Rg2. This circuit reduces the induced voltage due to circuit stray inductance.

![Triggering Circuit Diagram](image)

Figure 4.4: The Weis gate turn-off drive control circuit

The advantages of this topology include:

- A simple gate drive control circuit with few components and
- Operates only when Vce exceeds the Zener breakdown voltage, avoiding high turn-off loss, compared to pure resistive gate control.

The disadvantages incurred include:

- Only incorporates control for minimising the switching stress at turn-off and
- The voltage rating of the Zener diode has to be increased in high-voltage applications, resulting in the need to use several series connect Zener diodes.
4.3.2 M. Kimata et al.

The gate drive circuit shown in figure 4.5 focuses on reducing the turn-off surge voltage by varying the series gate resistance [4.5].

This gate drive circuit changes the gate resistance during turn-off, hence reducing the dL/dt which causes the overshoot voltage. The IGBT gate during the initial turn-off process is driven by gate resistor $R_{g1}$, as transistor Q3 bypasses resistor $R_{g2}$. If excessive negative dL/dt is detected across R4, transistor Q4 turns on which turns off transistor Q3. The gate resistance is increased as $R_{g1}$ is now in series with $R_{g2}$.

![Figure 4.5: Schematic of the Kimata dL/dt detection gate drive circuit](image)

The advantages of this topology include:

- Simple control circuitry and
- Additional detection or timing circuits are not required as the voltage across R4 is nearly proportional to the IGBT collector current.

The disadvantages incurred include:

- A modified IGBT is needed;
- Only incorporates control for minimising the switching stress at turn-off;
- The control circuit transistors are on during steady-state, resulting in unnecessary power loss; and
- Operates after the collector voltage has reached the supply level.
4.3.3 **S. Takizawa et al.**

The gate drive circuit shown in figure 4.6 enhances the switching performance of the IGBT through reducing the turn-off switching loss [4.6].

The gate drive control strategy is based on the control of the parallel connected gate resistors according to the shown logic table. The gate resistance is inversely varied according to the turn-off current level. The turn-off current level detection is via the $V_{ce(sat)}$ detector and diode $D_{sat}$ connected to the IGBT collector. The detected current is fed to the comparator circuit which parallel connects the necessary gate resistors to vary the gate resistance. At high turn-off current, the IGBT is switched with a higher gate resistance and the inverse applies at low current.

![Turn-off Current Detection Circuit](image)

Figure 4.6: Schematic of the Takizawa gate drive circuit and its turn-off logic table

The advantage of this topology includes:

- Flexibility in controlling the voltage stress by adjusting the number of parallel resistors.

The disadvantages incurred include:

- Fast and synchronised switching of the control switches in series with the parallel resistors, is required and
- Only applicable to the turn-off process.
4.3.4 J. Vinod et al.

The gate drive circuit shown in figure 4.7 optimises switching performance by applying three successive control stages to both switching transitions [4.7].

Stage one is initiated by turning on a MOSFET and the low resistance results in rapid charging/discharging of the input capacitance. In stage two, the MOSFET is switched off and a bipolar transistor is operated in the active region, thereby controlling the gate current. The gate current is reduced in this stage to limit \( \frac{dV_{ce}}{dt} \) and \( \frac{dI_c}{dt} \). Stage three involves a large gate current by switching on the MOSFET again, which rapidly completes the switching process and reduces the switching losses.

![Active Gate Drive Circuit Diagram](image)

Figure 4.7: Schematic of the Vinod active gate drive circuit

The advantages of this topology include:

- Control for minimising the switching stress at both turn-on and turn-off and
- Applicable in both hard-switched and soft-switched applications.

The disadvantages incurred include:

- The process is complicated and requires accurate feedback detection during the switching transient and
- Has to be tuned to a particular IGBT.
4.3.5 S. Musumeci et al.

The gate drive circuit shown in figure 4.8 is based on shaping the gate current in order to independently control the collector voltage and current gradients [4.8-4.9].

The gate drive operates by reducing the device switching times with intervention during the Miller effect period. The gate current is shaped with a pulse synchronised by the detection of the Miller zone. The gate drive consists of a conventional push-pull output stage with the addition of a current generator for a high current pulse at turn-on and a turn-off current sink, to improve the dynamic characteristics of the switching device. Injecting gate current pulses during the Miller period speeds up the collector voltage variation without changing the collector current gradient.

![Figure 4.8: Schematic of the Musumeci IGBT gate drive circuit](image)

The advantages of this topology include:

- Separate control of the collector voltage and current, thereby allowing the reduction of both power losses and electromagnetic interference (EMI) and
- The turn-off delay time can be varied, which allows the possibility of eliminating the underlap requirement in bridge leg configurations.

The disadvantages incurred include:

- Precise detection of the Miller zone is critical in order to minimise the energy losses. Thus each gate drive needs to be tuned to its individual switching device and
- Several control stages are required which results in complex circuitry.
4.3.6 S. Park et al.

The circuit diagram in figure 4.9 illustrates active gate control that independently controls IGBT $dV_{ce}/dt$ and $dI_i/dt$ [4.10].

Figure 4.9a shows the circuit to control the collector voltage rate during each switching transition. A small capacitor $C_M$ is connected between the IGBT gate circuit and the collector to sense the collector voltage variation during the switching transitions, and generates current feedback for $dV_{ce}/dt$ control. The emitter-coupled transistor pair, depending on $V_c$, determines the amount of reflected current delivered by the current mirror circuits to the IGBT gate.

Figure 4.9b shows the circuit for $dI_i/dt$ control. The small inductance $L_e$ in the IGBT emitter senses the $dI_i/dt$ during the switching transitions and generates a feedback voltage for the control circuit. The $dI_i/dt$ control method is similar to the $dV_{ce}/dt$ approach, where the measured $dI_i/dt$ is used to vary a dependent current source that extracts $I_f$ from the gate current.

The advantages of this topology include:

- Activate only during the transition stages;
- Self-synchronising; and
- Independent control of $dV_{ce}/dt$ and $dI_i/dt$ in hard-switching applications.
The disadvantages incurred include:

- All the transistors need to operate in the active region for a fast response, resulting in increased gate drive power and
- A separate circuit is required for each control function and transition stage, making the gate drive complicated.

4.3.7 M. Helsper et al.

The active gate drive circuit shown in figure 4.10 illustrates two-step gate resistor turn-off control and $dL/dt$ turn-on control [4.11].

The function of the two-step gate resistance control circuit is to vary the gate resistance during turn-off in order to control the collector voltage stress. The IGBT input capacitance is discharged through the low gate resistance $R_{g1(\text{off})}$ during the initial turn-off process and is switched to a higher value $R_{g2(\text{off})}$ when the desaturation detection diode $D_{\text{sat}}$ blocks. The $dL/dt$ control circuit depends on the measured $dL/dt$ and feeds additional current to the IGBT gate during the initial turn-on process in order to reduce the switching time. The $dL/dt$ circuit is deactivated when the $dL/dt$ is large and the IGBT gate current is via $R_{g(\text{on})}$. 

Figure 4.10: Helsper's gate drive control circuit for two-step resistor and $dL/dt$ control
The advantages of this topology include:

- Independent control of $dV_{ce}/dt$ and $dL/dt$ and
- Reduced turn-off delay time and a lower collector current gradient.

The disadvantages incurred include:

- A high-voltage rating diode, with series connection of several diodes, is required for $D_{sat}$ in high-voltage applications and
- Parameter temperature drift can cause high switching losses as control operation is based on the initial switching process.

### 4.4 IGBT Fault Protection

IGBT gate drive design involves resolving the tradeoff between switching losses and switching stresses. Apart from these design factors, the gate drive should have the ability to protect the IGBT under short-circuit and overvoltage conditions. Both conditions are usually unpredictable and a short duration stress of a few nanoseconds can results in device failure [4.2, pp. 229-245].

![IGBT Fault Conditions](image)

*Figure 4.11: IGBT fault conditions*

#### 4.4.1 Overvoltage protection

A high overvoltage is associated with a high $dI/dt$ in circuit stray inductance. The free-wheel diode snap recovery can also induce a high-voltage spike that exceeds the IGBT voltage rating. Some lower current IGBTs are avalanche rated but are not designed to operate in this mode continuously [4.23]. Overvoltage protection techniques use either active gate drive circuits [4.4-4.11] or non-linear impedance devices such as Zener diodes or varistors [4.2, pp. 238] to clamp the overvoltage, hence control the switching stress.

For non-linear impedance devices, the relationship between the current, $I$, and the voltage across its terminals, $V$, can be described by [4.2, pp. 239]:

---

76
\[ I = kV^\alpha \] 

(A) 

where \( k \) = a constant depending on device geometry 
\( \alpha \) = the degree of conduction non-linearity

A high value of \( \alpha \) produces a better clamping effect. The Zener diode, with typically \( \alpha = 35 \), is able to function as a constant voltage clamp as shown in figure 4.12. To avoid high power losses, the Zener diode is used in the collector-gate circuit.

Figure 4.12: The I-V characteristics of power Zener diodes and varistors [4.2, pp. 241]

i) **Non-linear impedance device - Zener diode**

As shown in figure 4.12, the Zener diode is an effective transient voltage suppressor that can be connected across the IGBT as shown in figure 4.13 for overvoltage protection.

Figure 4.13: Utilising a Zener diode for overvoltage protection

In the event of an overvoltage condition, the Zener diode \( D_z \) clamps the IGBT collector voltage by tending to turn on the device. Diode \( D_1 \) provides the current path for \( D_z \) but isolates the gate signal during on-state operation. Higher voltage application is possible with series connected Zener diodes.
The advantages of this topology include:

- Simple protection circuit that can be incorporated into the gate drive and
- Fast response time to random voltage transients.

The disadvantages incurred include:

- The number of Zener diode increases with higher voltage applications and
- The uncontrolled clamping by the Zener diode during an overvoltage condition may produce simultaneous turn-on of the IGBTs in a bridge leg, causing a short-circuit to the supply.

### 4.4.2 Short-circuit protection

The common IGBT failure mechanism during short-circuit is excessive power dissipation that results in a rapid junction temperature increase. High temperatures occur in high concentrated current locations due to non-uniformity of the dopant concentrations, leading to device destruction [4.12]. The ability of the gate drive to rapidly control or turn-off the IGBT within its short-circuit withstand time will prevent degradation of long term reliability [4.13]. Figure 4.14 illustrates the effect of gate voltage on short-circuit current and device withstand time. A modest reduction of gate voltage, \( V_g \), results in a decrease in the fault current and a significant improvement in the short-circuit withstand time, \( t_{sc} \).

![Figure 4.14: Variation of \( I_{sc} \) and \( t_{sc} \) as a function of gate voltage [4.13]](image-url)
Two types of short-circuit fault conditions [4.14] exist which require gate drive protection:

- Fault under load and
- Hard switching fault.

A fault under load occurs when the IGBT is subjected to a short-circuit during normal conduction. The fault causes the collector voltage to increase from its on-state level, resulting high $dV_{ce}/dt$ across the Miller capacitance. This induces a capacitive current into the gate, raising the gate-emitter voltage. As a consequence, the collector current increases to a peak depending on the IGBT characteristics and the gate drive parameters.

A hard switching fault occurs when the device is turned on into a fault. During the prefault stage, the device supports the full supply voltage. As such, the $dV_{ce}/dt$ produced by the IGBT is smaller than the fault under load case. The Miller effect has less influence since the Miller capacitance is much lower at high collector-emitter voltages and a lower fault current can be expected.

Three protection circuit topologies [4.15-4.20] are described to illustrate the limiting of IGBT fault current under a short-circuit condition.

i) R. Chokhawala et al.

The fault current limiting circuit shown in figure 4.15 lengthens the IGBT short-circuit withstand time by lowering the gate voltage [4.15-4.16].

The protection circuit uses collector-to-emitter voltage sensing to detect a short-circuit and subsequently lowers the gate voltage by switching on the MOSFET M1. The initial gate bias voltage of M1 is controlled by the time constant formed by the resistors and the MOSFET input capacitance during turn-on and is kept below its turn-on threshold voltage. In the event of a short-circuit, diode $D_{sat}$ is reverse biased causing the MOSFET gate voltage to increase. The selection of R1, R2, and R3 ensures the MOSFET is switched on under this condition. Once M1 is on, the IGBT gate voltage is clamped to the lower Zener diode voltage, $V_{Dz1}$. The fault current magnitude is decreased, thereby reducing the power dissipation in the IGBT.
The advantages of this topology include:

- Simple control circuit to reduce the fault current magnitude and
- Is capable of riding through a temporary fault by restoring the gate voltage to its normal on-state level. This prevents false tripping and shut down of the whole circuit.

The disadvantage incurred includes:

- The voltage rating of the sensing diode $D_{\text{sat}}$ depends on the IGBT operating voltage. A higher blocking voltage or several series connected diodes are required in high-voltage applications.

**ii) V. John et al.**

The fault protection circuit shown in figure 4.16 limits the gate voltage during a short-circuit, thereby reducing the power dissipated in the device [4.17-4.18].

Fast fault detection and limiting the fault current are essential features of the protection circuit. Fault current detection is based on two feedback signals, namely the collector desaturation voltage and the estimated collector current. The collector desaturation detection is via diode $D_{\text{sat}}$ connected to the IGBT collector which rapidly responds to a low impedance hard switching fault.

Collector current detection is through the voltage induced in the IGBT Kelvin connections at turn-on and is effective in detecting large inductive faults. In the event of a short-circuit, $Q_1$ is switched on causing $C_1$ to charge to the breakdown voltage of $D_{z1}$.
The gate voltage is reduced and clamped by $D_{z1}$. A precharge voltage control circuit is incorporated to charge $C_1$ to a level below the IGBT turn-on threshold voltage. This compensates for the delay in the protection circuit.

The advantages of this topology include:

- Fast detection and clamping of the fault current and
- Precise clamping of the fault current reduces power dissipation, thereby increasing the IGBT short-circuit withstand time.

The disadvantages incurred include:

- Several control stages are required to ensure precise detection and clamping of the fault current, making the protection circuit complicated;
- The selection of the breakdown voltage of $D_{z1}$ is dependent on the IGBT transconductance gain and this affects performance in a temperature varying environment;
- The voltage rating of $D_{sat}$ has to be increased in high-voltage applications and can results in series connection of several diodes in order to obtain the required voltage rating; and
- Access to IGBT cells to form Kelvin connections for current sensing is needed.
iii) *R. Pagano et al.*

The fault current limiting circuit shown in figure 4.17 limits the fault current peak by dynamic reduction of the gate resistance [4.19-4.20]

![Gate Voltage Control Circuit](image)

**Figure 4.17: Schematic of the Pagano gate voltage control circuit**

During fault conditions, the $dV_c/dt$ produced will cause a Miller capacitance current into the IGBT gate. This capacitive current is diverted into the gate-to-emitter capacitance, $C_{ge}$, and the capacitor $C1$ in the control circuit, which forward biases the PNP transistor Q2. With Q2 on, NPN transistor Q1 turns on and shunts the gate resistance. This action corresponds to the diversion of the induced Miller capacitance current from $C_{ge}$, reducing the gate-to-emitter voltage rise hence limiting the fault current produced.

The advantages of this topology include:

- Simple control circuitry and
- It is only active during the transient fault period.

The disadvantages incurred include:

- The selection of $C1$ is critical to ensure the protection circuit is not activated at IGBT turn-off due to the high spike voltage produced. Proper sizing of $C1$ to bias Q2 correctly has to be factored in a temperature varying environment and
- Not able to turn-off the IGBT without additional circuitry.
4.5 Summary

The IGBT switching process is similar to the voltage driven MOSFET except that the IGBT during turn-off has certain bipolar characteristics [4.21]. Conventional gate drive methods depend on fixed gate resistance to suppress EMI to an acceptable level while maintaining minimum switching losses and stresses [4.22]. To satisfy the switching stress constraint and EMI generated, the gate resistance can be large. However, this compromise leads to long switching times and higher switching losses. Thus circuit techniques are necessary to control the IGBT output dV_{c/dt} and dl_{c/dt}, to prevent high switching losses. In general, the main gate drive requirements, as summarised in figure 4.18, are:

- Be capable of driving short rise time currents into capacitive loads and maintaining a continuous output for PWM applications;
- Able to reduce the delay times at both turn-on and turn-off;
- Control or clamp overvoltage at turn-off;
- Provide a reverse bias voltage during the off-period to improve IGBT immunity to EMI noise and dv/dt transients; and
- Be electrically isolated from the IGBT power circuit.

Additional control features should also be incorporated. Overshoot and short-circuit protection for the IGBT are essential in preventing device and circuit destruction. Three main failure mechanisms occur that can result in IGBT failure:

- Exceeding the thermal limit;
- Latching; and
- Exceeding the voltage rating.

Fault currents increase device junction temperature and can cause thermal runaway. An IGBT may survive a short-circuit but fail when being turned-off. The fault clearing dI_{c/dt} can induce a high-voltage stress on the IGBT due to stray circuit inductance. Minimising stray inductance and slowing the rate of fall of the collector current by the protection circuit can avoid this failure mode. To efficiently protect the IGBT during overvoltage and short-circuit, the gate drive should possess the following features:
The ability to limit the peak fault current and thereby prolonging IGBT short-circuit withstand time;
- The fault detection circuit should be fast and insensitive to noise;
- The flexibility to vary the fault level trip point;
- Not affect the switching behaviour during normal IGBT operation; and
- At shutdown, the reducing fault current $dI/dt$ should be controlled to reduce the overvoltage stress.

Figure 4.18: Literature overview of gate drives

References


CHAPTER FIVE

The Active Gate Drive and its Design Methodology for Series Connected IGBTs

The active voltage control (AVC) technique in [5.1-5.2] demonstrated dV<sub>ce</sub>/dt control by providing a pre-determined reference signal, V<sub>ref</sub>, to the active gate drive circuit. The control circuit consists mainly of analogue circuitry to generate the reference signal and its associated pre-conditioning step [5.1]. The requirement of the pre-conditioning step is critical to ensure the control of IGBT dV<sub>ce</sub>/dt but its use contributes additional switching losses. Figure 5.1 shows the active gate drive circuit presented in [5.1] for fixed dV<sub>ce</sub>/dt control. The penalties incurred with this fixed technique are additional switching losses due to the pre-conditioning step and the dV<sub>ref</sub>/dt selection is based on the slowest switching device in the series chain. In general, the AVC in [5.1] is dependent on a:

- Fixed pre-conditioning step period and
- Fixed dV<sub>ref</sub>/dt based on the worse case switching device.

Figure 5.1: The active gate drive circuit [5.1]
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The IGBT modules used in the experiments are referenced by the manufacturer’s name, as shown in Table 5.1.

Figure 5.2 shows the experimental circuit used to expose the additional switching loss at turn-off due to the pre-conditioning gate voltage step. The switching losses in figure 5.3 parts (a) and (b) for the same $dV_{ce}/dt$, indicates a 25% turn-off loss increase with AVC. Figure 5.3c shows loss of $dV_{ce}/dt$ control when a higher $dV_{ref}/dt$ is fed to the gate drive, even with a prolonged pre-conditioning step in order to compensate for the switching delay.

Table 5.1: Manufacturer references for the IGBT modules

<table>
<thead>
<tr>
<th>IGBT Code</th>
<th>Current Rating (A)</th>
<th>Voltage Rating (V)</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSM75GAL120DN2</td>
<td>75</td>
<td>1200</td>
<td>Siemens</td>
</tr>
<tr>
<td>GP600DHB16S</td>
<td>600</td>
<td>1600</td>
<td>Mitel</td>
</tr>
</tbody>
</table>

Figure 5.2: Single-ended DC chopper circuit ($V_s = 100V_{dc}$)
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(a) AVC with $dV_{ce}/dt = 50V/\mu s$
(Siemens IGBT)

(b) Hard-switching with $dV_{ce}/dt = 50V/\mu s$
(Siemens IGBT)

(c) High $dV_{ce}/dt$ (Mitel IGBT)

Figure 5.3: Illustration of AVC additional switching loss and the loss of $dV_{ce}/dt$ control at IGBT turn-off

Unless the IGBTs are matched, their parameter tolerances will require that different preconditioning step periods are used to overcome switching delay variations. These associated switching losses can be minimised for devices that have lower input capacitance. In addition, the strong voltage dependence of the output capacitance [5.3] will affect $dV_{ce}/dt$ control as a fixed $dV_{ce}/dt$ may not be able to compensate output capacitance changes due to temperature variations [5.4] or a sudden collector voltage...
increase during redundancy (a device failure) voltage redistribution. In bridge leg applications, the free-wheel diode reverse recovery snap can cause IGBT failure [5.5]. A fixed controlled turn-on $dV_{ce}/dt$ effectivelyovercomes this failure but may face limitations at higher conducting currents [5.6].

The limitations associated with the AVC presented in [5.1] are summarised as:

- The fixed pre-conditioning step period at turn-off, required for compensating switching delays, incurs additional switching loss, $P_d$, due to the $V_{ce}$ voltage step before the fall of the collector current, $I_c$, as shown in figure 5.4. IGBT parameter spread, along with temperature effects, increases the voltage step duration. The fixed period pre-conditioning step extends into the Miller region where the IGBT is in a quasi turn-off state. A higher switching loss results.

![Figure 5.4: Illustration of increased switching loss](image)

- The $dV_{ref}/dt$ applied to the active gate drive circuit depends on the response of the slowest IGBT. The device output capacitance is the main parameter that determines the required $dV_{ref}/dt$ for $dV_{ce}/dt$ control. As this capacitance is collector voltage dependant, a fixed $dV_{ref}/dt$ will suffer from higher switching losses or poor $dV_{ce}/dt$ control when the IGBT collector voltage varies as shown in figure 5.5.
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Free-wheel diode snap recovery in a bridge leg results in a collector voltage oscillation on the complementary IGBT during the turn-on process, as shown in figure 5.6. A slow turn-on $dV_{ce}/dt$ on the commutating IGBT is able to suppress this voltage oscillation but with a fixed turn-on $dV_{ref}/dt$, the voltage oscillation may appear when the conducting current is increased.

Figure 5.6: Induced voltage oscillation due to free-wheel diode snap recovery

An active gate drive technique, similar to [5.1], is proposed in this chapter to overcome the limitations described. The proposed gate drive has the ability to:
- Reduce the pre-conditioning step additional losses;
- Compensate $dV_{ce}/dt$ due to temperature variation and redundancy; and
- Prevent failure due to free-wheel diode reverse recovery overvoltage (see Chapter 7).

Figure 5.7 illustrates the proposed design methodology for AVC of series connected IGBTs in medium-voltage drives and details the function and objective of each control block of the active gate drive.

![Gate drive design methodology for series connected IGBTs](image)

**Figure 5.7: Gate drive design methodology for series connected IGBTs**

### 5.1 Control Principles for Dynamic and Static Voltage Sharing

Series connection of IGBTs requires voltage sharing across each device in order to prevent overvoltage failure. There are two stages within the switching cycle that have to be addressed to prevent voltage failure, namely:

- Dynamic (or transient) voltage sharing and
- Static (or steady-state) voltage sharing.

Static voltage sharing can be achieved by connecting identical resistors across each switching device [5.7]. The same resistors can also be used as part of the voltage divider used for the collector feedback voltage signal shown in figure 5.1. The dual role of these parallel resistors reduce circuit design complexity and improve system efficiency.
Although this approach is used, the dynamic voltage sharing aspect is the primary focus of the design methodology.

Figure 5.8 illustrates the concept of dynamic voltage sharing for three series connected IGBTs. Apart from the $dV_{ce}/dt$ control provided by the active gate drive, each $dV_{ce}/dt$ can be individually varied to ensure voltage balance independent of parameter variations or redundancy conditions. Initial $dV_{ce}/dt$ tracking is based on the slowest switching IGBT in order to ensure all switching devices track. Subsequent $dV_{ce}/dt$ increase is attempted when all devices are able to track the reference signal. In the event of any one device not being able to achieve $dV_{ce}/dt$ tracking, the $dV_{ref}/dt$ is reduced to the previous rate. The flexibility of varying $dV_{ref}/dt$ minimises the switching losses associated with $dV_{ce}/dt$ control, which is limited by the characteristics of the slowest device.

Figure 5.9 shows the control blocks and their functional objectives to achieve AVC. The scheme consists of two different controllers that generate and determine the necessary $dV_{ref}/dt$. These two controllers are classified as a local gate controller and a global controller.

The main function of the local gate controller is to generate the reference voltage, $V_{ref}$, with a minimum pre-conditioning step period and ensure the IGBT $dV_{ce}/dt$ is controlled. The global controller determines if all the series connected IGBTs are able to track the present $V_{ref}$ and communicates to each local gate controller to either increase, maintain or decrease its $dV_{ref}/dt$ in order to maintain $dV_{ce}/dt$ control.
The communications interfacing technique for both controllers is based on fibre optic communications so as to obtain a high isolation breakdown voltage, which is critical in medium to high voltage designs. The design methodology for the proposed AVC technique is presented in three parts.

- Local gate controller circuit
- Global controller circuit
- Interfacing between controllers

The function and objective of each part are now detailed with low-voltage experimental results to illustrate the design approach.

**Figure 5.9: Block diagram of the control circuitry**

### 5.2 Local Gate Controller Circuit

The basis of the AVC technique involves closed loop voltage control of the active gate drive and the IGBT collector voltage, during the Miller region. The primary function of the local gate controller is to ensure that the IGBT \( dV_{cc}/dt \) follows the reference \( dV_{ref}/dt \) and to adjust the duration of the pre-conditioning step for minimum switching losses.
Figure 5.10 shows the block diagram of the local gate controller. The $V_{\text{ref}}$ signal generation is dependent on the control algorithm programmed in the FPGA, the signal from which is converted and amplified by the DAC and instrumentation amplifier. The controlled IGBT gate voltage is determined from the differential amplifier comparison of the generated $V_{\text{ref}}$ and IGBT feedback collector voltage, $V_{\text{fd}}$. Feedback from the differential amplifier output to the FPGA provides $dV_{ce}/dt$ control detection. In summary, the function and objective of the local gate controller is to:

- Generate and vary the reference signal slope to the gate drive;
- Vary the pre-conditioning step period to maintain minimum switching losses; and
- Detect the effectiveness (error) of $dV_{ce}/dt$ control.

![Block diagram of the local gate controller](image)

**5.2.1 Description of the closed loop voltage control approach**

The gate circuit closed loop voltage control is based on the differential amplifier function shown in figure 5.11a.

During ideal turn-off conditions, $\alpha dV_{ce}/dt = dV_{\text{ref}}/dt$. This produces $V_{\text{out}}$ and $I_g$ as shown in figure 5.11b (shaded portion). However when $\alpha dV_{ce}/dt$ is lower than $dV_{\text{ref}}/dt$, $dV_{out}/dt$ becomes smaller, resulting in lower $dI_g/dt$. With $I_g$ more negative, $C_{gc}$ discharges faster, thereby forcing $dV_{ce}/dt$ to follow $dV_{\text{ref}}/dt$. In the case of $\alpha dV_{ce}/dt$ being higher than $dV_{\text{ref}}/dt$, $dV_{out}/dt$ becomes larger, resulting in higher $dI_g/dt$. This slows the discharge of $C_{gc}$, thereby reducing $dV_{ce}/dt$ and enabling the collector to follow the reference. Closed loop voltage control is based on varying $I_g$ during the Miller region, according to the difference between $V_{ce}$ and $V_{\text{ref}}$. 

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5.2.2 Description of the adaptive control used to minimise switching losses

Additional switching losses are incurred with AVC due to the pre-conditioning step used to bring the device into the active region and the selection of \( \frac{dV_{ref}}{dt} \), both of which are based on the slowest IGBT. The proposed active gate drive is able to vary both parameters, using adaptive control to minimise the switching losses. That is, adaptive control of:

- The pre-conditioning step duration and
- The \( \frac{dV_{ce}}{dt} \) variation.

i) Adaptive control of the pre-conditioning step duration

A pre-conditioning step is required in the reference signal to bring the device into the active region before the \( \frac{dV_{ref}}{dt} \) occurs [5.1]. However, this step incurs switching losses, especially when the step duration is extended so as to give active region operation. The ideal period for the pre-conditioning step is such that the collector just enters the active region, where the input capacitance has been charged to the threshold level. If this step period is fixed, higher switching losses may be produced due to the spread of IGBT parameters \( (t_{d(off)}, C_{gc}) \) among the series connected devices. An increase in switching losses results in an increase in operating temperature. The pre-conditioning step brings the
IGBT further into the active region since IGBT switching delay times decrease with temperature. An adaptive control approach, illustrated in figure 5.12a, is implemented to reduce the step period at turn-off in order to maintain a constant minimum switching loss for AVC operation.

(a) Illustration of adaptive step control for turn-off

(b) Diagram of the adaptive control approach

Figure 5.12: Adaptive control features of the local gate controller
The output of the differential amplifier, $V_{out}$, is sampled during the turn-off transition. By enabling the D-latch at a specific level, dynamic information is fed back to the FPGA for processing. Once the switching device starts to respond to the pre-conditioning step, $V_{out}$ increases. The sampled data at point 1 in figure 5.12b will determine the required pre-conditioning period in order to maintain minimum loss. As long as the average sample data is below the threshold level specified in the control algorithm, the step period remains unchanged. A step period reduction occurs once the threshold level is exceeded.

The current design only incorporates adaptive control with a single change to the step period at turn-off. Adaptive control at turn-on is not implemented since the IGBT input capacitance is low and the step period is short. A single Mitel IGBT under AVC is connected in a DC chopper circuit with a 100Vdc supply voltage, as shown in figure 5.13. Figure 5.14 shows the practical results for the adaptive control approach. The purpose of this experiment is to illustrate a reduction in pre-conditioning step period when the turn-off switching loss is increased due to a reduction of $R_g$. Varying $R_g$ will simulate the parameter spread of the switching devices, in terms of switching delay time, and the temperature affects that result in increased switching loss.

![Active Voltage Control](image)

Figure 5.13: Experimental circuit for adaptive control of the pre-conditioning step period
Figure 5.14: Experimental results for the adaptive control approach

Figure 5.14a shows the reference pre-conditioning step based on a gate resistance of 30Ω. The high clock frequency (100MHz) and sampling rate (20MHz) of the FPGA and ADC results in the voltage spikes seen at the differential amplifier output, V_{out}. With R_g = 30Ω, the period of the step voltage for V_{ce} is 2μs. As R_g is reduced to 23Ω, simulating the parameter spread or temperature effect, the IGBT switching delay time decreases and the period for the step voltage seen in figure 5.14b is increased to 3.5μs. A further reduction of R_g to 22Ω causes the adaptive control to reduce the pre-conditioning step to 4μs in order to maintain the V_{ce} step voltage duration at 2μs, as shown in figure 5.14c. The
reduced step period returns the step voltage seen on $V_{ce}$ to its original period, thereby minimising the switching loss. This control process is accomplished by average data sampling during interval $\Theta$ in figure 5.12b.

ii) $dV_{ce}/dt$ variation

The $dV_{ce}/dt$ variation control depends on the feedback data during interval $\Theta$ in figure 5.12b. When the scaled $dV_{ce}/dt$ is equal to $dV_{ref}/dt$, the output voltage, $V_{out}$, from the differential amplifier will produce a relatively constant voltage level (error). In the event that $dV_{ce}/dt$ is slower, this constant voltage level will fall. The FPGA control is based on the sampled data within this window, and reduces the $dV_{ref}/dt$ in order to enforce $dV_{ce}/dt$ control. The current practical design incorporates adaptive control on $dV_{ce}/dt$ variation at the turn-off transient only, in order to demonstrate the control process. The same adaptive control approach is applicable to the turn-on transition. With reference to figure 5.13, with $R_g = 22\Omega$, figure 5.15 shows the experimental results with a single Mitel IGBT, experiencing $dV_{ce}/dt$ variation. An external snubber circuit is connected in parallel to the IGBT in order to simulate a loss of $dV_{ce}/dt$ control, as shown in figure 5.15b.

Part (b) of figure 5.15 indicates the reduction of $V_{out}$ within the transition period when the snubber circuit is activated. The FPGA responds by decreasing the $dV_{ref}/dt$ in order to maintain $dV_{ce}/dt$ control as shown in figure 5.15c. The ability to vary $dV_{ce}/dt$ enables the series connected IGBTs to be switched at the fastest possible rate for minimum switching loss while still maintaining $dV_{ce}/dt$ control.
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(a) $dV_{ce}/dt$ control is maintained

\[ \frac{dV_{ref}}{dt} = 2V/\mu s \]

(b) With snubber circuit

\[ \frac{dV_{ref}}{dt} = 2V/\mu s \]

(c) With snubber but reduced $dV_{ref}/dt = 1.5V/\mu s$

Figure 5.15: Experimental results for adaptive control with $dV_{ce}/dt$ variation

5.3 Global Controller Circuit

The role of the global controller circuit is to monitor $dV_{ce}/dt$ control status from each local gate controller and then instruct all the local gate controllers to either increase the $dV_{ref}/dt$ in order to minimise the switching loss, or maintain or reduce the slope to enforce $dV_{ce}/dt$ control. The process of $dV_{ref}/dt$ selection is shown in figure 5.16, for three series connected IGBTs.
The initial dV_{ref}/dt demand sent to each local gate controller, (S0, S1 = 0), is the slowest in order to ensure that dV_{ce}/dt control is achieved by all switches. If all local gate controllers maintain dV_{ce}/dt control, (S0 = 1, S1 = 0), the dV_{ce}/dt demand is increased in the next switching cycle in an attempt to minimise the switching loss. If dV_{ce}/dt control is maintained, the global controller will demand a higher dV_{ref}/dt from the local gate controllers. However when one or more local gate controllers are not able to maintain dV_{ce}/dt control, (S0 = 0, S1 = 1), the dV_{ref}/dt demand is lowered to its previously level. For illustrative purposes, the present FPGA implementation allows three different dV_{ref}/dt for both turn-off and turn-on (nonadaptive), as shown in figure 5.17.

![Diagram](image)

**Figure 5.16: Selection of dV_{ref}/dt by the global controller**

<table>
<thead>
<tr>
<th>Selection of V_{ref}</th>
<th>dV_{ref}/dt Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>S1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

/ indicates dV_{ce}/dt control is achieved
X indicates loss of dV_{ce}/dt control

![Diagram](image)

**Figure 5.17: Turn-off and turn-on dV_{ref}/dt’s**

The experimental results in figures 5.18 and 5.19 demonstrated the three different rates for turn-off and turn-on, respectively. The dV_{ce}/dt variation in this experiment uses a low supply voltage to illustrate the basic control concept.
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Figure 5.18: Turn-off $dV_{ce}/dt$ variation

(a) $t_fv = 5\mu s$

(b) $t_fv = 6\mu s$

(c) $t_fv = 9\mu s$

Figure 5.19: Turn-on $dV_{ce}/dt$ variation

(a) $t_fv = 4\mu s$

(b) $t_fv = 5\mu s$

(c) $t_fv = 7\mu s$
5.4 Interfacing between the Global and Local Gate Controllers

In order for the global controller to monitor tracking performance and issue the appropriate \( V_{\text{ref}} \) command for \( dV_{oc}/dt \) control, it bidirectionally communicates digitally with the local gate controllers. The interface has to provide adequate electrical isolation and a wide bandwidth for data transfer in a medium to high voltage system. Typical electrical isolation techniques involve a transformer-based approach or optical isolation [5.8]. The traditional disadvantages of transformer-based isolation are limited bandwidth, poor common mode noise immunity, and constructional isolation problems at high voltages (>11kV). Optical isolation, such as an optocoupler, utilises a light-emitting diode (LED) transmitter and a photo-transistor receiver to convey information across an isolated barrier. Optocouplers are an effective (below 10kV), low cost method of isolating signals and eliminate common transformer disadvantages. Furthermore, optics allows DC signals to be transferred. Table 5.2 compares transformer-based isolation and optical isolation.

<table>
<thead>
<tr>
<th>Transformer-based Isolator</th>
<th>Optical Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Requires large PCB areas as isolation voltage</td>
<td>High isolation voltage is achievable with in small area</td>
</tr>
<tr>
<td>increases</td>
<td></td>
</tr>
<tr>
<td>Poor common-mode transient immunity</td>
<td>Good common-mode transient immunity, especially with fibre optic link</td>
</tr>
<tr>
<td>Suitable only for AC signal</td>
<td>Suitable for both AC and DC signals</td>
</tr>
<tr>
<td>Does not require an additional voltage source to</td>
<td>Additional voltage source is needed to reconstruct the isolated signal</td>
</tr>
<tr>
<td>reconstruct the isolated signal</td>
<td></td>
</tr>
<tr>
<td>Magnetic characteristics are highly dependent on</td>
<td>Electrical characteristics of receiving transistor are highly temperature dependent</td>
</tr>
<tr>
<td>the physical structure</td>
<td></td>
</tr>
<tr>
<td>The data rate is constrained by</td>
<td>The data rate is constrained by the photo-transistor charge/discharge time</td>
</tr>
<tr>
<td>signal attenuation due to transformer leakage</td>
<td></td>
</tr>
<tr>
<td>inductance</td>
<td></td>
</tr>
</tbody>
</table>
Optocouplers with isolation properties above a few kV tend to have long, temperature dependent, propagation delays, with highly asymmetrical switching times. At voltages in excess of 5kV, fibre optic approaches are preferred. Apart from the higher transmission rates with lower losses and lower error rates, fibres allow higher voltage isolation between the controllers. The advantages of using fibre communications include:

- Extremely wide bandwidth;
- Immunity to EMC;
- Rugged construction;
- Ease of expansions of system capability; and
- High electrical isolation.

Figure 5.20 shows the control blocks for the fibre optic link. As optical isolation is provided by the fibre optic link (glass/plastic), a LED transmitter and a photo-transistor receiver are required to convert the information.

In the proposed design, each local gate controller reference signal must be synchronised. This is achieved with the control signals from the global controller as shown in figure 5.21.
In figure 5.22, synchronism is degraded when the transmitter is subjected to temperature variations. As the optical power of the transmitter is directly proportional to the LED anode current, $I_A$, a temperature increase will reduce the LED voltage drop, $V_A$, thereby increasing $I_A$ [5.9].

An off-the-shelf fibre optic package from Agilent Technologies, consisting of a transmitter (HFBR-1521), a receiver (HFBR-1524), and a plastic fibre optic link capable of 1MBd, are used in figure 5.23 to highlight fibre optic limitations in a temperature varying environment. Figure 5.24 shows the experimental delay results for the control signal, as the transmitter and receiver case temperatures are increased independently.
Figure 5.24: Variation of the propagation delay, \( t_{pd(LH)} \) and \( t_{pd(HL)} \), as transmitter and receiver case temperatures are increased separately.

Figure 5.24a shows a 40ns reduction of the control signal propagation delay when the transmitter case temperature is increased from 19°C to 70°C. Unless compensated this characteristic will result in control signal synchronisation degradation.
Possible solutions to overcome this limitation include:

- Placement of all the transmitters and their associate interface circuitry in the same temperature environment and
- Utilise a constant current source for the transmitter interface circuit to maintain a constant anode current to the LED.

The temperature effect on the transmitter will however, increase the propagation delay of the high to low signal transition as shown in figure 5.24b. This is due to the increased minority carrier lifetime in the LED. This device dependant characteristic is difficult to eliminate with compensation circuits. The rising edge will behave as shown in figure 5.24a. This is due to the reduced diode voltage drop and increased LED current. This feature may be mitigated by means of a constant current drive. Receiver case temperature variations do not vary the propagation delay before the low to high signal transition in figure 5.24c. This is due to the constant optical power transmitted by the transmitter. However, the same delay effect for a high to low signal transition (in figure 5.24b) is shown in figure 5.24d. The increased photo-transistor temperature results in an increased minority carrier lifetime. The falling edge compared to the rising edge of the control signal, with increased case temperature, results in a lower propagation delay (88ns vs 320ns), smaller delay variation (15ns vs 40ns), and faster transition time (14ns vs 80ns).

Although the trailing edge is preferable for synchronisation, the present design requires synchronisation of the local gate controller be triggered on the rising edge, which has better possibilities for temperature stabilisation. In addition, all the transmitters are placed next to each other and hence will experience the same temperature variations. The absolute delay variation at high-temperature (40ns) is small and is not critical since the IGBT response is much slower. With the transmitter optical power controlled, increased receiver temperature will not affect the control signal rising edge (figure 5.24c). Table 5.3 summarises the propagation delay variation due to the 51°C temperature increase. The general propagation delays, with respect to the optical power for both the transmitter and receiver, are shown in figure 5.25.

<table>
<thead>
<tr>
<th>Device Subjected to Hot Air</th>
<th>Temperature Variation (ΔT)</th>
<th>Rising Edge [tpd(LH) = 360ns]</th>
<th>Falling Edge [tpd(HL) = 78ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>51°C</td>
<td>-40ns</td>
<td>+15ns</td>
</tr>
<tr>
<td>Receiver</td>
<td>51°C</td>
<td>0</td>
<td>+10ns</td>
</tr>
<tr>
<td>Both Devices</td>
<td>51°C</td>
<td>-40ns</td>
<td>+25ns</td>
</tr>
</tbody>
</table>
5.4.1 Effects of signal delay

PSpice simulation analysis was conducted on two series connected IGBTs, in a DC chopper circuit, with a skew time delay $\Delta t$ in the reference signal $V_{\text{ref}}$, to evaluate the effects of jitter. The results are shown in figure 5.26.

Figure 5.26b shows turn-off of two series IGBTs when the reference for S2 is delayed by 2.6$\mu$s. Although there is an overshoot voltage on S1, AVC actively clamps the voltage once it reaches 124Vdc. This occurs since $V_{\text{ref}}$ reaches its off-level, which cause the differential amplifier output voltage to turn-on IGBT S1 (see Chapter 7.5). Figure 5.26c shows the voltage overshoot sustained by S1 due to a time delay between the reference signals. AVC is able to maintain $dV_{\text{dc}}/dt$ control with long $\Delta t$ delays. A 20% voltage overshoot is only observable when $\Delta t \geq 2.2\mu$s. Importantly, there is no significant voltage overshoot when the delay is less than 200$\mu$s. Thus delay variations (40$\mu$s) due to fibre optic temperature effects will not affect dynamic voltage sharing.
Chapter Five: The Active Gate Drive and its Design Methodology for Series Connected IGBTs

Vs = 200Vdc
20mH
10Ω

Vs

Vref(S1)

Vref(S2)

AVC

S1

R_s

Vce(S1)

Vref(S2)

AVC

S2

R_s

Vce(S2)

(a) Circuit diagram

(b) Active clamping at Δt = 2.6μs

(c) Graphical plot of Vce(S1) with respect to Δt

Figure 5.26: PSpice simulation results for two series connected IGBTs with time delay in Vref
5.5 Summary

i) Design approach for the controllers

An extension of the AVC presented in [5.1] has been described, which overcomes the limitations of the earlier controller. The analogue circuit used to generate the reference ramp, is replaced by a digital method which uses an FPGA, DAC, and instrumentation amplifier. A digital approach allows simple adaptive control of the pre-conditioning step period and $dV_c/dt$ variations. Table 5.4 indicates the relatives features of the digital and analogue approaches.

Table 5.4: Features of an analogue approach [5.1] and the proposed digital approach, for $V_{ref}$ generation

<table>
<thead>
<tr>
<th>Analogue Approach [5.1]</th>
<th>Digital Approach</th>
</tr>
</thead>
<tbody>
<tr>
<td>- The $V_{ref}$, (pre-conditioning step period and $dV_{ref}/dt$), is dependent on parameter values of each gate drive. Physical changes are necessary to change $V_{ref}$</td>
<td>- The $V_{ref}$, (pre-conditioning step period and $dV_{ref}/dt$), is based on the control algorithm within the FPGA, thus does not require hardware changes to change $V_{ref}$</td>
</tr>
<tr>
<td>- The AVC involves analogue circuitry which increases reliability to noise at high-voltages</td>
<td>- Even with a gate drive digital ground, careful component layout is necessary to minimised ground noise levels</td>
</tr>
</tbody>
</table>

FPGA technology is used rather than a DSP for the global and local gate controllers as it provides abundant input/output pins and offers parallel processing without complex algorithms. A comparison between an FPGA and a DSP technological approach is shown in Table 5.5.
Table 5.5: Comparison between FPGA and DSP controllers

<table>
<thead>
<tr>
<th>FPGA</th>
<th>DSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Flexible architecture based on a logic block concept that offers a wide variety of logic functions</td>
<td>• Flexibility is restricted by program execution time</td>
</tr>
<tr>
<td>• Design flexibility and configurable adaptability with optimal utilisation can minimise space and power</td>
<td>• DSPs lack flexibility</td>
</tr>
<tr>
<td>• Single chip parallel structures and arithmetic algorithms are inherent</td>
<td>• Few concurrent tasks tend to be serialised for processing</td>
</tr>
<tr>
<td>• Can operate at higher sampling rates (100MHz), especially when combined with rigid, repetitive tasks</td>
<td>• Operate at low sampling rates and high complexity</td>
</tr>
</tbody>
</table>

The FPGA is programmed using a schematic capture approach [5.10]. The schematic has lower-level macros (schematic-based modules and state machine modules) which allow signal transitions within the algorithm to be monitored during the design stage, ensuring the synchronisation of specific signals. High-level hardware description languages, such as Verilog and VHDL, can be used for posting once the control principle of each stage has been finalised. The control flow, for the local gate and global controllers, is illustrated in the flowcharts in figure 5.27.
Detect control signal from Global Controller (Rising Edge)

Control Signal?

Yes

Activate Counters to Generate Required \( \frac{dV}{dt} \)

Detect the Dynamic Information on \( V_n \) for Adaptive Control

Pre-conditioning Step Period

Threshold Exceeded?

No

Yes

Reduced Counts for the Step Period

Maintained Counts for the Step Period

\( \frac{dV}{dt} \) Variation

Threshold Reduced?

Yes

Enable the Loss of \( \frac{dV}{dt} \) Control Signal to Global Controller

No

Indicate to Global Controller that \( \frac{dV}{dt} \) Control is Achieved

(a) Local gate controller

Issue the Slowest \( \frac{dV}{dt} \) to each Local Gate Controller Upon Power up

During AVC Operation

Detect the \( \frac{dV}{dt} \) Control Signals from each Local Gate Controller

Is \( \frac{dV}{dt} \) control achieved by all Local Gate Controllers

Yes

\( \frac{dV}{dt} \) Control?

No

Increase \( \frac{dV}{dt} \) (until Maximum)

Reduce \( \frac{dV}{dt} \) (till Minimum)

(b) Global controller

Figure 5.27: The control flow for both controllers


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### ii) Initial pre-conditioning step period

The local gate controller is able to vary the pre-conditioning step interval and feedback the \( dV_{ce}/dt \) control status to the global controller. The initial pre-conditioning step is necessary to overcome the IGBT switching delay time and bring it into the active region before \( dV_{ce}/dt \) operation starts. An adequate step period is needed in the reference signal to ensure closed loop voltage control. However, a prolonged duration will result in additional switching loss, while an inadequate step will not result in \( dV_{ce}/dt \) control. Different IGBTs require a different pre-conditioning period. To determine the preferred step period, apart from the switching delay time, \( t_d \), the initial gate-collector capacitance discharge/charging time needs to be considered.

For turn-off \( dV_{ce}/dt \) control, the initial gate-collector capacitance, \( C_{gc1} \), at turn-off is large, as shown in figure 5.28. Reducing the initial capacitance discharge time, \( t_{Cgc1} \) will enhance the effectiveness of AVC, as the active gate drive is able to control \( dV_{ce}/dt \) without incurring a significant capacitive delay. Typical manufacturer datasheets do not specify \( t_{Cgc1} \), as the gate-collector capacitance is non-linear and dependent on the collector voltage. Although the initial pre-conditioning interval can be determined practically, an adaptive method is possible, similar to the \( dV_{ce}/dt \) variation approach. A worse case initial pre-conditioning step is applied to the reference signal during the first switching transition. This is gradually reduced until \( V_{out} \) (figure 5.11a) no longer remains low. However the current design is based on experimental adjustment to determine the initial preferred pre-conditioning step period for the IGBT.

![Typical gate-collector capacitance plot](image)

**Figure 5.28: Typical gate-collector capacitance plot**
Figure 5.29 illustrates the approach used in the present design for determining the initial pre-conditioning interval for turn-off $dV_{ce}/dt$ control. The turn-on step period is dominated by the switching delay time ($t_{d(on)}$) as the gate-collector capacitance is small at high voltage. As such, the adaptive control is not necessary, nor implemented for the turn-on period.

The turn-off pre-conditioning interval in the present design can be reduced when the additional switching loss at turn-off exceeds the specified threshold level in the local gate controller. The features of adaptive control of the pre-conditioning step period, compared to the constant step period in [5.1], are indicated in Table 5.6.

Table 5.6: Features of a constant pre-conditioning period and an adaptive pre-conditioning step

<table>
<thead>
<tr>
<th>Constant Step Period [5.1]</th>
<th>Adaptive Control on Step Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Switching loss increases as the IGBT threshold voltage decreases due to a temperature increase</td>
<td>• Switching loss is minimised by the adaptive control process</td>
</tr>
<tr>
<td>• Physical re-tuning of the gate drive is necessary when replacing IGBTs due to device parameter tolerances</td>
<td>• Control determines the preferred initial step period without physical re-tuning</td>
</tr>
</tbody>
</table>
iii) IGBT $dV_{ce}/dt$

The collector voltage rate of rise/fall will determine the IGBT switching losses. AVC for series connected IGBTs requires the $dV_{ref}/dt$ to match the slowest device. However, a fixed $dV_{ref}/dt$ may not maintain $dV_{ce}/dt$ control or may incur higher than necessary switching loss when the device is capable of tracking a higher $dV_{ref}/dt$. Table 5.7 indicates the features of IGBT $dV_{ce}/dt$ adaptive control and constant $dV_{ref}/dt$ as in [5.1].

Table 5.7: The features of adaptive $dV_{ref}/dt$ and constant $dV_{ref}/dt$ control in [5.1]

<table>
<thead>
<tr>
<th>Constant $dV_{ref}/dt$ [5.1]</th>
<th>Adaptive $dV_{ref}/dt$</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Fixed switching loss based on the slowest IGBT in the series chain</td>
<td>- Switching loss minimised as the switching rates are constantly adjusted to the highest rate achievable by all devices</td>
</tr>
<tr>
<td>- Gate drive parameters must be match to each IGBT</td>
<td>- The switching rate is maintained at a maximum, independent of the IGBT</td>
</tr>
<tr>
<td>- Not able to distribute IGBT voltage stress after redundancy (failure)</td>
<td>- The reference magnitude can be increased to cater for redundancy voltage redistribution after IGBT short-circuit failure</td>
</tr>
</tbody>
</table>

iv) Conclusion

The AVC approach for series connected IGBTs in [5.1] has been extended. Additional control features are incorporated into the active gate drive to improve its efficiency. The control stability relating to the active gate drive is presented in [5.10], not within this chapter. Figure 5.30 shows an overview of the presented AVC method for the series connection of IGBTs.
Chapter Five: The Active Gate Drive and its Design Methodology for Series Connected IGBTs

Active Voltage Control

Active Gate Drive Circuit

Local Gate Controller
- Ramp Circuit
- Gate Drive Circuit
- \( V_{ce} \) Monitoring Circuit

Chapter 5.2

Global Controller
Chapter 5.3

Interfacing Technique (Fibre Optics)
Chapter 5.4

Adaptive Control on Pre-conditioning Period
Chapter 5.2.2i

Monitoring of Local Gate Controller \( dV_{ce}/dt \) Control

Selection of \( dV_{ref}/dt \)

Transmitter/Receiver

Fibre Optic Link

Adaptive Control on \( dV_{ce}/dt \) Variation
Chapter 5.2.2ii

Limitation

Loss of Synchronism at High-Temperature

Figure 5.30: Overview of the features in the proposed AVC

References


Chapter Five: The Active Gate Drive and its Design Methodology for Series Connected IGBTs


CHAPTER SIX

Practical Results for Series Connected IGBTs

With series IGBT operation, well-matched gate drives will not ensure balanced dynamic voltage sharing between the switching devices. Rather it is IGBT parasitic capacitances, mainly gate-collector capacitance \( C_{gc} \), that dominate transient voltage sharing. As \( C_{gc} \) is collector voltage dependant and is significantly larger during the initial turn-off transition, it dominates IGBT dynamic voltage sharing. With reference to the circuit diagram in figure 6.1, the results in figure 6.2 show the Orcad PSpice simulation analysis of the effect of \( C_{gc} \) (simulated by \( C_M \)) on collector-emitter voltage displacement, \( \Delta V_{ce} \), during turn-off.

Although the \( C_M \) variation is in the tens of picofarad range, the \( \Delta V_{ce} \) variation is significant, as shown in figure 6.2. This indicates the importance of matching \( C_{gc} \) in series connected IGBTs in order to achieve balanced dynamic turn-off voltage sharing.

![Figure 6.1: PSpice schematic used to illustrate the \( C_{gc} \) (\( C_M \)) effect](image)

\( V_s = 150Vdc \)
Figure 6.2: Effect of $C_M$ on $\Delta V_{ce}$

Figure 6.3 shows two series connected, hard-switched IGBTs with the same gate drive parameters ($V_{ge(on)} = +15V$, $V_{ge(off)} = 0V$, $R_g = 5\Omega$). The turn-off dynamic voltage sharing of each IGBT is shown in figure 6.4.

Figure 6.3: Two series connected IGBTs with matched gate drives
Figure 6.4: The effect of \( C_{eg} \) on turn-off dynamic voltage sharing

(a) Gate signals with \( V_s = 0 \)

(b) Gate signals with \( V_s = 200\text{Vdc} \)

(c) Collector-emitter voltage sharing

Figure 6.4: The effect of \( C_{eg} \) on turn-off dynamic voltage sharing

(1:20 attenuated voltage differential probe)

Figure 6.4a shows each IGBT gate voltage without any supply voltage, \( V_s = 0 \). Both gate voltages have the same response time for turn-off. When \( V_s \) is 200Vdc, a 30ns shorter Miller period is observed for S1, in figure 6.4b. This results in the imbalanced turn-off transient voltage sharing shown in figure 6.4c.

Several experiments, outlined in figure 6.5, are conducted using the proposed AVC method on different IGBT modules, to demonstrate its effectiveness in achieving dynamic voltage sharing of series connected IGBTs. The experiments are based on two and three
series devices operating at scaled down voltages ($V_s$ less than 300Vdc) and currents so as to safely illustrate the control features described in Chapter 5. The experiments include:

- Adaptive control of the pre-conditioning step period;
- Adaptive control on $dV_{ce}/dt$ variation;
- AVC effectiveness with respect to load current variation; and
- Active clamping with respect to IGBT tail current effects.

Figure 6.5: Overview of the experiments conducted

The IGBT module types used are shown in Table 6.1 and IGBT addressing is based on the manufacturer’s name. The circuit free-wheel diode is the 1200V, 50A internal anti-parallel diode in the Siemens IGBT package BSM50GAL120DN2.

Table 6.1: Manufacturer’s reference for the IGBT modules

<table>
<thead>
<tr>
<th>IGBT Code</th>
<th>Current Rating (A)</th>
<th>Voltage Rating (V)</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSM75GAL120DN2</td>
<td>75</td>
<td>1200</td>
<td>Siemens</td>
</tr>
<tr>
<td>GP200MHS12</td>
<td>200</td>
<td>1200</td>
<td>Dynex</td>
</tr>
<tr>
<td>GP600DHB16S</td>
<td>600</td>
<td>1600</td>
<td>Mitel</td>
</tr>
</tbody>
</table>
6.1 Series Operation using Siemens IGBTs

A 200Vdc voltage supply is used in conjunction with two series connected Siemens IGBTs to demonstrate AVC principles. Three experiments, as outlined in figure 6.6, are conducted to analyse AVC effects on dynamic voltage sharing, dV_{ce}/dt variation, and the synchronisation gate delay technique introduced in Chapter 3.5.1.

![Two Series Connected Siemens IGBTs](image)

**Figure 6.6: The experiments involving Siemens IGBTs**

6.1.1 Turn-off dynamic voltage sharing

Figure 6.7 shows a DC chopper circuit switched by two series connected Siemens IGBTs. The average load current, I_L, is 1A and the case temperature of both IGBTs is maintained at 21°C. Figure 6.8 illustrates AVC effectiveness at turn-off, based on its comparison with uncontrolled hard-switching.

![Experimental circuit using Siemens IGBTs](image)

**Figure 6.7: Experimental circuit using Siemens IGBTs**
Chapter Six: Practical Results for Series Connected IGBTs

6.1.2 \(dV_{ce}/dt\) variation - Siemens IGBTs

Chapter 5.3 illustrated AVC ability to vary IGBT \(dV_{ce}/dt\) during switching transitions. Based on the circuit in figure 6.7, figures 6.9 and 6.10 show three different \(V_{ce}\) rates at turn-off and turn-on. The limitations related to the selection of the \(V_{ref}\) rate (voltage rise and fall times) at turn-off and turn-on are outlined in Chapter 6.5.1.

Significant imbalanced voltage sharing, \(\Delta V = 12.5\%\) of \(V_s\), is observed in figure 6.8a with uncontrolled hard-switching. This highlights the necessity for series connected IGBTs to be controlled during transitions in order to prevent excessive high collector voltage stresses. Figure 6.8b shows AVC ability to achieve balanced dynamic turn-off voltage for both series devices (\(\Delta V = 1.25\%\) of \(V_s\)).

(a) Uncontrolled hard-switching

(b) AVC switching

Figure 6.8: Comparison between turn-off dynamic voltage sharing with AVC and uncontrolled hard-switching
Chapter Six: Practical Results for Series Connected IGBTs

Figure 6.9: Turn-off dVce/dt variation

Figure 6.10: Turn-on dVce/dt variation
Chapter Six: Practical Results for Series Connected IGBTs

The three $V_{ce}$ rates are chosen to illustrate AVC effectiveness to control $dV_{ce}/dt$ variation and maintaining dynamic voltage sharing, as shown in both figures. The voltage error, $\Delta V$, shown in figure 6.9a, is due to the IGBT tail current mismatched, which will be investigated in Chapter 6.4.

6.1.3 Synchronised gate delay technique

The synchronisation technique [6.1] depends on matched gate signal timings for each series devices. The practical circuit in figure 6.11 was used to determine method effectiveness for two series connected Siemens IGBTs. The gate signals are delayed relative to one another in order to achieve dynamic voltage sharing. The dynamic voltage sharing for the series IGBTs before and after gate delay implementation is shown in figure 6.12, with $V_s = 100$Vdc and $I_L = 0.75$A. Device static voltage balancing utilises resistor networks across each collector-emitter terminal.

![Test circuit for evaluating the synchronised gate delay technique](image)

Figure 6.11: Test circuit for evaluating the synchronised gate delay technique
Chapter Six: Practical Results for Series Connected IGBTs

(a) Turn-off – before delay implemented

(b) Turn-off – after delay implemented

Figure 6.12: Synchronisation test circuit results – with and without signal delay
(1:20 attenuated voltage differential probe)

In figure 6.12a, S1 turns off before S2 due to its lower parasitic gate-collector capacitance. This causes a significant (80%) turn-off overshoot voltage difference between the two devices. With a delay of 480ns on $V_{ge(S1)}$, dynamic voltage sharing is significantly improved, $\Delta V$ decreasing from 80% to 20%, as shown in figure 6.12b. This technique is further analysed for potential application in areas involving current variation (AC application) and temperature variation (prolonged operating time).

i) Load current variation - AC application

With reference to the circuit in figure 6.11, the load current, $I_L$, is varied so as to study the turn-off effect with current variation, on two series connected devices. $V_{ge(S1)}$ is delayed to achieve balanced dynamic voltage sharing and the delay time is then fixed. With $V_S = 200V_{dc}$ and a device case temperature of $T_c = 21^\circ C$, the results in figure 6.13 show voltage sharing with a load current variation.
Figure 6.13: The effect of load current variation with fixed synchronisation gate control

Figure 6.13a shows balanced voltage sharing during turn-off. As $I_L$ increases (figure 6.13b), a time difference, $\Delta t$, of 40ns is observed between the two devices, thus showing imbalanced dynamic voltage sharing. The dynamic response of a switching device varies with load current.

Referring to the equations in reference 6.2, pp. 366-382, the turn-off delay time $t_{d\text{ (off)}}$ and IGBT transconductance $g_m$ are related by:

$$t_{d\text{ (off)}} = R_g (C_{ge} + C_{gc}) \ln \left( \frac{V_g}{V_{g(th)} + I_l/g_m} \right)$$  \hspace{1cm} (s) \hspace{1cm} (6.1)

$$g_m = \mu_{ns} C_{ox} \frac{Z}{L} \left( V_g - V_{g(th)} \right)$$  \hspace{1cm} (S) \hspace{1cm} (6.2)

where $\mu_{ns}$ = surface mobility of electrons within the MOSFET structure

$Z/L$ = width/length of the MOSFET conduction channel

$$C_{ox} = \frac{\text{dielectric constant}}{\text{gate oxide thickness}}$$  \hspace{1cm} (F) \hspace{1cm} (6.3)
From these equations, \( g_m \) is not constant and is dependant on the gate oxide capacitance \( C_{ox} \). As \( C_{ox} \) is determined by gate oxide thickness \( t_{ox} \), which varies between IGBT devices and \( g_m \), \( t_{d(off)} \) will be different for each IGBT. If the \( g_m \) variation is small, \( \Delta t \) will be relatively small, as seen in figure 6.13b. But with the addition of temperature variation, \( \Delta t \) increases as \( g_m \) is temperature dependent [6.3].

**ii) Case temperature variation - prolonged operating time**

Using the test circuit in figure 6.11, the case temperature, \( T_c \), of both IGBTs is increased by forced hot air. This simulates prolonged IGBT operation at increased load current and temperature conditions. The result is shown in figure 6.14. The peak load current, \( I_L \), at the turn-off transition is 1.8A and the temperature is increased from \( T_c = 21^\circ C \) to \( 41^\circ C \).

![Figure 6.14: The effect of a case temperature increase of 20°C (T_c = 41°C)](image)

The result indicates that a time delay of 20ns occurs when the case temperature for both IGBTs is increased by 20°C. Increased temperature reduces IGBT gate threshold voltage [6.4]. Unless the IGBTs are matched, each will respond differently to temperature variations. In the experiment conducted, S1 responds faster than S2 with the 20°C temperature increase, thereby causing imbalanced dynamic voltage sharing. Although the gate signal delay time can be increase for S1, this will pose several problems due to:
The delay implemented will have to increase as temperature increases. However based on a pre-determined variable duty cycle, there will be a delay limit applicable to the gate signal and
Continual delay time variation due to both temperature and current is required and this may result in high frequency AC application limitations.

The net effect of increased load current and temperature is cumulative.

### 6.2 Series Operation using Dynex IGBTs

Figure 6.15 outlines the experiments conducted with two series connected Dynex IGBTs at \( V_s = 200\text{Vdc} \). The \( \frac{dV_{ce}}{dt} \) variation and the effect of load current variation on AVC are considered.

![Figure 6.15: Experiments involving Dynex IGBTs](image)

#### 6.2.1 \( \frac{dV_{ce}}{dt} \) variation - Dynex IGBTs

Figures 6.16 and 6.17 show three different rising and falling \( V_{ce} \) rates during switching, for the DC chopper shown in figure 6.7 with \( I_L = 1.8\text{A} \).

The results demonstrate AVC effectiveness in controlling \( V_{ce} \) rates. The voltage error, \( \Delta V \), shown in figure 6.16a, is due to IGBT tail current mismatched, which will be investigated in Chapter 6.4. In each case, AVC is able to maintain \( \frac{dV_{ce}}{dt} \) control with different transition rates. \( V_{ref} \) rate limitations at turn-off and turn-on are considered in Chapter 6.5.2.
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Figure 6.16: Turn-off transition
(a) $t_r = 760\,\text{ns}$
(b) $t_r = 1\,\mu\text{s}$
(c) $t_r = 2\,\mu\text{s}$

Figure 6.17: Turn-on transition
(a) $t_f = 800\,\text{ns}$
(b) $t_f = 1.5\,\mu\text{s}$
(c) $t_f = 3\,\mu\text{s}$
6.2.2 **Load current variation - Dynex IGBTs**

Using the circuit in figure 6.7, the load current is increased from 1.8A to 9A by reducing the load resistance, $R_L$. Figure 6.18 shows AVC effectiveness when the load current is increased.

![Figure 6.18: Load current effect on AVC](image)

(a) $t_{rv} = 760\text{ns} \ (I_L = 9\text{A})$

(b) $t_{rv} = 1\mu\text{s} \ (I_L = 9\text{A})$

(c) $t_{rv} = 2\mu\text{s} \ (I_L = 9\text{A})$

The increased load current does not affect $dV_{ce}/dt$ control for the Dynex IGBTs with different $V_{ce}$ rates. However, the voltage error in the tail current period, $\Delta V$, as observed in figure 6.18a, increases with load current and is considered in Chapter 6.4.
6.3 Series Operation using Mitel IGBTs

The AVC experiments at $V_s = 300$Vdc involving three series connected Mitel IGBTs are shown in figure 6.19. Adaptive control of $dV_{ce}/dt$ variation and the pre-conditioning step considered in Chapter 5.2.2, are investigated in the experiments.

Figure 6.19: Experiments with Mitel IGBTs

6.3.1 $dV_{ce}/dt$ variation - Mitel IGBTs

Figure 6.20 shows the test circuit, with three series connected Mitel IGBTs, used on a 300Vdc supply rail. The results in figures 6.21 and 6.22 show the AVC switching transitions for three different $V_{ce}$ rates, at $\bar{I}_L = 1.5$A. Limitations related to $V_{ref}$ rate at turn-off and turn-on are described in Chapter 6.5.3.

Figure 6.20: Test circuit with three series connected Mitel IGBTs
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Figure 6.21: Turn-off transition

Figure 6.22: Turn-on transition
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With a common $V_{\text{ref}}$ to all three IGBTs, AVC is able to maintain dynamic voltage sharing, as shown in figures 6.21 and 6.22. Automatic AVC adjustment of $V_{\text{ref}}$ when poor $dV_{ce}/dt$ control occurs, is shown in figure 6.23. An external snubber, $C_s$, is connected across S3 to simulate poor $dV_{ce}/dt$ control.

![Figure 6.23: AVC of $dV_{ce}/dt$ variation](image)

In figure 6.23, the snubber limits S3 $dV_{ce}/dt$ during turn-off under AVC operation. Thus the voltage across S3 does not track $V_{\text{ref}}$, causing imbalanced voltage sharing before the activation of AVC with adaptive control. Poor $dV_{ce(S3)}/dt$ control results in a reduction of $V_{\text{ref}}$ to the next slower rate for all the IGBTs in order to regain dynamic voltage sharing. Each IGBT controller constantly monitors and adjusts $dV_{ce}/dt$ performance when IGBT $dV_{ce}/dt$ control is lost. The latency for the AVC to change the $V_{\text{ref}}$ rate is estimated at 4µs. This latency is based on the time taken for the feedback signal to be sent from the local gate controller to the global controller and the subsequent change of the $V_{\text{ref}}$ rate, instructed by the global controller, to each local gate controller. The voltage overshoot after AVC with adaptive control is due to IGBT tail current magnitude and decay time differences.

6.3.2 Adaptive control of pre-conditioning step - Mitel IGBTs

The performance of the adaptive control described in Chapter 5.2.21 is demonstrated in figure 6.24. The control feature is sequentially activated on each IGBT in order to reduce the $V_{ce}$ step voltage duration at turn-off. The average load current is maintained at 1.5A and $t_{rv} = 4$µs.
Figure 6.24a shows a 2μs $V_{ce}$ step voltage duration, $\Delta t$, for all three IGBTs without adaptive control. A reduction of the step duration to 1.2μs occurs for S1 as AVC reduces its pre-conditioning step period. Similarly in part (b) and (c) of figure 6.24, adaptive control of each IGBT pre-conditioning step reduces each $V_{ce}$ step voltage duration to 1.2μs. Dynamic voltage sharing and the reference point for the $V_{ce}$ ramp are independent of the adaptive control.
6.3.3 **Load current variation - Mitel IGBTs**

Using the circuit in figure 6.20, the load current is progressively increased by reducing the load resistance, $R_L$. The results in figure 6.25 show the effect of load current variation on turn-off, and illustrate AVC effectiveness in AC applications.

![Figure 6.25: Effect of load current variation on three series connected IGBTs](image)

(a) $I_L = 2.8A$  
(b) $I_L = 19A$

Dynamic voltage sharing of the three IGBTs is not affected by load current. Both parts of figure 6.25 demonstrated AVC effectiveness in controlling IGBT dynamic voltage sharing. The error voltage, $\Delta V$, increases at higher load current due to increased IGBT tail current differences.

### 6.4 IGBT Tail Current Effect

The error voltage, $\Delta V$, highlighted in Chapter 6.1, 6.2, and 6.3, is caused by variations in tail current characteristics [6.5-6.6]. Mismatched tail currents results in the device with the lower tail current charge supporting a higher voltage and incurring a higher switching loss. AVC is not effective in the tail current region since the device is no longer in the active region. Using the circuit in figure 6.3 with snubber controlled switching, this phenomenon is shown in figure 6.26 for two series connected Mitel IGBTs.
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Figure 6.26a shows matched dynamic voltage rise sharing with $C_s = 3\text{nF}$. However, imbalanced voltage sharing occurs during the tail current interval. This effect is dependent on IGBT tail current characteristics and larger snubber capacitance compensates this error voltage, as shown in figure 6.26b. The capacitance for voltage control during the tail current period poses a similar problem to that for series connected diodes, where differences in reverse recovery charge occur. The capacitor must be sized such that it can absorb the charge associated with tail current mismatch, without an excessive voltage rise. The task is complicated by the fact that the IGBT tail current is often poorly characterised.

Two series connected AVC controlled IGBTs, like in figure 6.7, are used to illustrate the IGBT tail current effects with respect to different operating conditions, as outlined in figure 6.27.
6.4.1 Static balancing resistance variation - IGBT tail current effect

The static balancing resistance, $R_s$, across each IGBT in figure 6.7 is varied to determine its effects on the error voltage during the tail current interval. The average load current and device case temperature are maintained at 0.9A and 21°C respectively. Figure 6.28 shows the result for three different $R_s$ values.

![Figure 6.28: Turn-off voltage with $R_s = 1\, \Omega$, 6k$\Omega$, and 15k$\Omega$](image)

Figure 6.27: Experiments exploring the IGBT tail current effect
In figure 6.28, $\Delta V$ is 40V with $R_s = 15k\Omega$ and reduced $R_s$ decreases $\Delta V$. From equation 3.1, the difference in the tail current, $\Delta I_T$, is equivalent to the leakage current in $R_s$. Hence the static voltage sustained by one IGBT will be:

$$V_{DI} = \frac{V_s + (n-1)R_s\Delta I_T}{n}$$  \hspace{1cm} (V)  \hspace{1cm} (6.1)

where $n = \text{number of series devices}$

If $\Delta I_T$ is not zero, the error voltage will decrease as $R_s$ is reduced. The static resistance will thereby dominate the error voltage during the tail current interval. The main concern with low $R_s$ is the resultant increased power rating requirement. Alternatively, parallel capacitance can be added, in the form of an RC snubber.

### 6.4.2 Load current variation - IGBT tail current effect

With $R_s = 15k\Omega$ in figure 6.7, the load resistance, $R_L$, is progressively reduced to determine the load current effect on the error voltage supported by the IGBTs, as shown in figure 6.29.

The error voltage, $\Delta V$, increases as the load current, $I_L$, increases. This is due to the IGBT minority carrier recombination lifetime differences associated with the tail currents and is illustrated in figure 6.30. The IGBT that has the shortest recombination lifetime will sustain a higher voltage overshoot during the tail current interval, as $R_s$ in parallel will
support a higher voltage due to its higher current flow. The tail current difference, $\Delta I_T$, for two series connected IGBTs can be described by [6.2, pp. 478]:

$$\Delta I_T = \alpha_{pnp1} I_L \left( e^{-\frac{1}{\tau_{HL1}}} - e^{-\frac{1}{\tau_{HL2}}} \right)$$  \hspace{1cm} (A) \hspace{1cm} (6.2)

does this assume $\alpha_{pnp1} = \alpha_{pnp2}$ otherwise

$$\Delta I_T = \alpha_{pnp1} I_L e^{-\frac{1}{\tau_{HL1}}} - \alpha_{pnp2} I_L e^{-\frac{1}{\tau_{HL2}}}$$

where $\tau_{HL} = $ IGBT recombination lifetime

This implies that $\Delta I_T$ is proportional to $I_L$ and an increase in $I_L$ will increase the tail current difference.

![Diagram of IGBTs](image)

**Figure 6.30:** The tail current fall for two series connected IGBTs with difference pnp section recombination lifetimes
6.4.3 Device case temperature variation - IGBT tail current effect

IGBT S2 in figure 6.7 is subjected to a temperature increase and the error voltage supported is measured, with an average load current of 0.9A. Figure 6.31 shows the results at three different case temperatures for two series connected IGBTs.

In figure 6.31, S2 case temperature is varied while S1 case temperature is maintained constant at 22°C. Switch S2 has a shorter recombination lifetime than S1. Increasing S2 case temperature, hence increasing ΔT, increases S2 recombination lifetime, resulting in a reduced error voltage, ΔV. This means negative feedback occurs on the error voltage sustained by the shorter recombination lifetime device, as its junction temperature increases due to a higher switching loss.

6.4.4 AVC effects on error voltage - IGBT tail current effect

Although negative feedback exists on the error voltage with respect to device case temperature, the AVC technique is able to reduce ΔV. This active clamping process is described in Chapter 7.5. Using the circuit in figure 6.7, two series connected Dynex IGBTs illustrate the effects of AVC on ΔV. The results in figure 6.32 show the ΔV supported with snubber controlled switching and AVC switching.
Figure 6.32: Experimental results of snubber controlled switching and AVC clamping, on ΔV

Figure 6.32a shows ΔV = 70V with snubber control and the dVce/dt is similar to the AVC switching in figure 6.32b (200V/μs). Although dynamic voltage sharing is achieved, IGBT tail current decay time differences result in a high ΔV. External control cannot minimise this error voltage unless a high snubber capacitance is used, which results in slower switching (see figure 6.26). In figure 6.32b, ΔV is reduced with AVC clamping. The higher collector voltage at turn-off activates AVC, which causes gate turn-on. This transfers voltage to the series counter-part. Although tracking is lost during the tail current period, AVC acts to clamp the voltage overshoot. Larger system gains or smaller gate resistance in the gate drive will shorten the AVC clamping response time but may cause control system instability (see Chapter 7.5.1).

6.5 Analysis of \( V_{\text{ref}} \) Rate Limitations

Different \( V_{\text{ref}} \) rates, which the AVC is able to track, will be shown for the three IGBT modules (Siemens, Dynex, and Mitel). The fastest turn-off \( V_{\text{ref}} \) rate applicable to each IGBT is limited by either or both:

- IGBT device characteristics and/or
- AVC gate drive parameters.
The turn-on $V_{\text{ref}}$ rate is dependent on free-wheel diode recovery charge. This is illustrated and described in Chapter 7.4.2.

### 6.5.1 Siemens IGBT’s

As shown in figure 6.33, hard-switching the matched devices in the circuit in figure 6.3, achieves $t_r = 220\text{ns}$ (450V/μs). The fastest AVC turn-off $dV_{ce}/dt$ for the Siemens IGBT is $t_r = 320\text{ns}$ (310V/μs), with a $V_{\text{ref}}$ rate = 600ns and $I_L = 1.8\text{A}$, as shown in figure 6.9a. AVC is restrained by the gate drive which cannot produce a $V_{\text{ref}}$ rate of less than 600ns (for $t_r < 320\text{ns}$), as the instrumentation amplifier output voltage is slew rate limited. This hardware limitation is described in Chapter 6.6.

![Figure 6.33: Two matched, series connected Siemens IGBTs, hard-switched](image)

### 6.5.2 Dynex IGBT’s

The fastest turn-off $dV_{ce}/dt$ for the Dynex IGBT is $t_r = 760\text{ns}$ (130V/μs), with a $V_{\text{ref}}$ rate = 1.16μs and $I_L = 1.8\text{A}$, as shown in figure 6.16a. The $V_{\text{ref}}$ rate for $dV_{ce}/dt$ variation depends on AVC ability to maintain tracking at low load current. This is illustrated with the single IGBT DC chopper circuit shown in figure 6.34. Figure 6.35 shows $dV_{ce}/dt$ tracking at $V_s = 100\text{Vdc}, I_L = 0.26\text{A}$.
Figure 6.34: A single IGBT DC chopper circuit with AVC

Figure 6.35: \( \frac{dV_{ce}}{dt} \) tracking at \( I_L = 0.26 \text{A} \) (\( R_L = 311 \Omega \), \( V_{ref \ rate} = 1.16 \text{p} \)).

Figure 6.36a shows \( t_v = 400 \text{ns} \) (250V/μs) for the hard-switched Dynex IGBT at \( I_L = 0.86 \text{A} \). However AVC switching at \( t_v = 400 \text{ns} \) indicates poor \( \frac{dV_{ce}}{dt} \) tracking, as shown in figure 6.36b. A load current increase, figure 6.36c, allows AVC \( \frac{dV_{ce}}{dt} \) tracking only during the final part of the turn-off transition. From the results obtained, IGBT output capacitance (\( C_{gc} + C_{ce} \)) limits \( \frac{dV_{ce}}{dt} \). A higher load current allows a faster \( V_{ref \ rate} \) rate for a shorter \( t_v \) during the turn-off transition. This is confirmed by the circuit in figure 6.37, as time is inversely proportional to load current (\( \Delta t = C_{gc} \Delta V_{ce}/I_{gc} \) ).
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(a) Hard-switching at $I_L = 0.86A$

(b) AVC switching at $I_L = 0.86A$

(c) AVC switching at $I_L = 5.8A$

Figure 6.36: $dV_{ce}/dt$ at $t_v = 400ns$

Figure 6.37: IGBT parasitic capacitances affect AVC $V_{ref}$ rate

\[ I_L = I_{gc} + I_{ce} \]

\[ I_L = C_{gc} \frac{\Delta V_{ce}}{\Delta t} + I_{ce} \]
6.5.3 Mitel IGBT’s

The fastest turn-off d\(V_{ce}/dt\) for the Mitel IGBT is \(t_v = 4\mu s\) (25V/\(\mu s\)), with a \(V_{\text{ref}}\) rate = 7\(\mu s\) and \(I_L = 3A\), as shown in figure 6.21a. Hard-switching with the circuit in figure 6.34 and \(R_L = 100\Omega\), achieves \(t_v = 1.86\mu s\) (53V/\(\mu s\)), as shown in figure 6.38.

The same chopper circuit is used to test:
- Higher \(V_{\text{ref}}\) rate at different load currents and
- Higher \(V_{\text{ref}}\) rate at higher operating voltages.

![Figure 6.38: Hard-switched single Mitel IGBT with \(V_s = 100V_{dc}\), \(I_L = 0.86A\)](image)

i) Higher \(V_{\text{ref}}\) rate at different load current

AVC tracking is observed in figure 6.39 with a \(V_{\text{ref}}\) rate of 2\(\mu s\) (\(t_v = 1.5\mu s\), (66V/\(\mu s\))) and a feedback gain \(\alpha\) of 0.08. Figure 6.39a shows poor d\(V_{ce}/dt\) tracking at low load current (\(I_L = 0.84A\)). However increasing \(I_L\) to 6.5A as in figure 6.39b, indicates that the AVC attempts d\(V_{ce}/dt\) tracking during the final part of the transient. This is observed in Chapter 6.5.2 for the Dynex IGBT.
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Figure 6.39: $V_{ref}$ rate of 2μs with different load current, $V_s = 100$Vdc

ii) Higher $V_{ref}$ rate at higher operating voltage

The operating voltage for the circuit in figure 6.34 is increased to $V_s = 200$Vdc ($V_{ref}$ rate = 2μs, $\alpha = 0.04$). Figure 6.40a shows poor AVC tracking at $I_L = 1$A. However $dV_{ce}/dt$ tracking is achieved when the load current is increased to $I_L = 5$A (figure 6.40b). This contradicts the results in figure 6.39 when $V_s = 100$Vdc.

Figure 6.40: $V_{ref}$ rate at 2μs with $V_s = 200$Vdc
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Two conclusions can be drawn for the Mitel IGBT:

- The IGBT output capacitance affects $V_{\text{ref}}$ rate selection, as low load current limits $dV_{ce}/dt$ tracking and
- At higher operating voltages, the output capacitance (in particular $C_{gc}$) tends to decrease as the transition approaches the turn-off steady-state. As such, AVC can $dV_{ce}/dt$ track at higher $V_{\text{ref}}$ rates.

Selection of the fastest turn-off $V_{\text{ref}}$ rate for the Mitel IGBT is based on the particular operating voltage and lowest possible load current where AVC is able to track its $dV_{ce}/dt$.

6.6 Hardware Limitations

The main AVC limitation is additional switching loss, due to the pre-conditioning step and $V_{\text{ref}}$ rate determined by the slowest switching device. Adaptive control on the pre-conditioning step allows the switching loss to be minimised and $dV_{ce}/dt$ variation ensures $dV_{ce}/dt$ control is maintained.

In the current design in figure 6.41, the local gate controller instrumentation amplifier slew rate limits the $V_{\text{ref}}$ rate. The $V_{\text{ref}}$ rate limitation is shown in figure 6.42.

![Figure 6.41: DAC and instrumentation amplifier within the local gate controller](image)

Figure 6.41: DAC and instrumentation amplifier within the local gate controller
Parts (a) and (b) of figure 6.42 show the $V_{\text{ref}}$ rate generated when $t_{\text{DAC}} = 400\text{ns}$. The instrumentation amplifier produces a ramp rate of 600ns (18V/\mu s). A reduction of $t_{\text{DAC}}$ to 200ns, figure 6.42c, results in the distortion observed in figure 6.42d. This is due to the slew rate limitation of the instrumentation amplifier. A higher slew rate instrumentation amplifier is needed if a shorter $V_{\text{ref}}$ rate is required.
6.7 Summary

Three different IGBT modules have been used to demonstrate AVC effectiveness in controlling dynamic voltage sharing and the control features described in Chapter 5. A direct approach to achieve balanced dynamic voltage sharing using gate drive synchronisation \([6.1]\) was considered, with load current and case temperature variation limitations highlighted. Unlike the synchronisation technique, the proposed AVC technique is able to operate with the above varying conditions, without loss of dynamic voltage sharing of the series connected IGBTs.

The IGBT tail current characteristics are critical for series operation as they affect voltage sharing. Most AVC techniques described in Chapter 3 depend on balancing resistance \(R_s\) to circumvent the imbalance voltage but this incurs a higher power rating for the resistor. The proposed AVC technique clamps the imbalance voltage and transfers this voltage to a series counter-part, without resorting to lower \(R_s\). AVC simplifies the heat transfer issue related to the static balancing resistor network.

Figure 6.43 shows the overview of the experiments conducted to illustrate AVC effectiveness, with two and three series connected IGBT devices.
Figure 6.43: Overview of the experimentation based on the proposed AVC technique
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References


CHAPTER SEVEN

Active Voltage Control of Series Connected Free-wheel Diodes

In high-power applications, series connected semiconductor devices have the advantages over multi-level approaches of providing redundancy and more compact interconnections, hence simplifying system architecture which reduces stray inductance. Series connection of IGBTs for the voltage-source inverter has been well researched [7.1-7.7], unlike the associated series connected anti-parallel diodes commonly used for commutation in inverters. Most of the literature on series connected IGBTs involves either active voltage control (AVC) or load side control techniques. The principle of AVC [7.1-7.4] involves control of the gate current of each series device to achieve dynamic voltage balancing while load side control techniques [7.5-7.7] normally depend on snubber circuits to indirectly enforce dynamic voltage balancing. As AVC techniques avoid the use of additional power circuits, they allow a smaller and more flexible system architecture. However, most AVC techniques do not consider the reverse voltage balancing of anti-parallel diodes when used as commutating devices in bridge leg applications. This shortfall may prove critical in series connections when AVC techniques are employed. This chapter presents the AVC technique as functionalised in figure 7.1, which apart from being able to achieve dynamic voltage balancing for series connected IGBTs, is able to control voltage sharing effects of the anti-parallel free-wheel diodes.

Figure 7.1: The affect of AVC on free-wheel diodes during reverse recovery

7.1 Diode Reverse Recovery

A common limitation with free-wheel diodes (FWDs) is snappy recovery during the reverse recovery phase [7.8-7.13], resulting in high-voltage oscillations with excessive overshoot. Ongoing technology advancement on power diodes includes utilising alternative structure components and silicon carbide. Wide band-gap materials have
received increased attention because of their superior reverse recovery characteristics [7.14-7.16]. Hence a dramatic performance improvement has been projected for power switches when silicon is replaced by silicon carbide [7.17-7.18]. However, many technological barriers have yet to be overcome before silicon carbide power switches evolve for high-temperature, high-power applications [7.19]. Until such time, the failure modes associated with Si FWD snappy recovery need to be addressed, especially in high-power applications. When FWDs are connected in series, dynamic imbalance voltage sharing among the devices occurs due to differing reverse recovery characteristics. These conditions may eventually damage the anti-parallel connected IGBT. Matching of diode recovery characteristics is impractical given the high temperature dependence of reverse recovery.

Steady-state voltage sharing uses a resistor connected in parallel with each device as considered in Chapter 3. The method is simple and effective. The common technique considered in Chapter 3.4 for transient voltage balancing of series connected diodes, is to utilise parallel connected RC snubbers [7.20]. Theoretically pure capacitance is sufficient but resistance is added to decrease current magnitudes and to absorb some stored energy thereby damping any voltage oscillations. Technically the RC snubber approach is attractive since the snubber performs transient protection for both the switch and its anti-parallel diode. If this technique is applied to an AVC system, AVC advantages are diminished, bringing the system closer to a load side control approach.

Possible fault conditions should also be factored into the system design to prevent catastrophic failure to the series connected devices. Snappy recovery of FWDs is a common failure mechanism, and may lead to excessive voltage overshoot. Several factors contribute to this failure condition and include high commutating $di/dt$ and circuit stray inductance.

The equation for the total recovery stored charge, $Q_T$, in the diode drift region can be described by [7.11]:

$$Q_T = q A_{\text{eff}} \int n_e(x) \, dx = I_F \tau_{\text{eff}}$$

(7.1)

where

- $q$ = electron charge
- $A_{\text{eff}}$ = diode effective area
- $n_e(x)$ = excess minority carrier concentration
- $I_F$ = forward current
- $\tau_{\text{eff}}$ = minority carrier effective lifetime
In [7.11], the authors have indicated that the gradient of the excess carrier concentration at each side of the junction determines if the diode will suffer from snappy recovery. Equation (7.2) specifies if the depletion layer formed will result in snappy recovery, \((K > 1)\):

\[
K = \frac{n_e(p^+n^-)}{n_e(n^-n^+)} = \frac{n_e(d^-)}{n_e(d^+)}
\]  
(7.2)

\(K\) is the ratio of the excess carrier concentration at each side of the junction [7.11].

The voltage build-up phase during reverse recovery commences once the space charge layer within the \(n^-\) base region starts to widen. Soft recovery requires the avoidance of the sudden disappearance of excess minority carriers during the recovery process. Figure 7.2a illustrates single-sided controlled penetration of the depletion layer while removing the excess carriers from the anode when \(K < 1\). Soft recovery can be achieved under this condition as the excess carrier profile tends to slow down the spreading of the depletion layer. Figure 7.2b illustrates two-sided penetration of the depletion layer with excess carriers removed from both sides when \(K > 1\). Snappy recovery results from this condition as the final excess carriers are removed suddenly.

From equation (7.2), the excess carrier concentration at each junction side differs in time and with equation (7.1), the rate of change of the forward current, \(dI_F/dt\), will have considerable affect on the possibility of snappy recovery.

(a): Single-sided penetration of the depletion layer when \(K < 1\)
(b): Two-sided penetration of the depletion layer when \(K > 1\)

Figure 7.2: Excess minority carrier distribution during reverse recovery [7.11]
7.2 Theory of Voltage Sharing during Reverse Recovery

Diodes are series connected to increase the reverse blocking voltage when the source voltage is larger than that for any single device. Before a conducting string of series diodes can reverse block the source voltage, the diodes must recover from their reverse recovery charge flow. Figure 7.3 shows the theoretical imbalanced voltage sharing between two series connected diodes when they have different reverse recovery charge requirements. Both devices experience the same reverse dI_R/dt because the devices are in series. The slope of the reversing current is determined by the supply and the stray inductance:

\[
\frac{dI_R}{dt} = \frac{V_s}{L_{\text{stray}}} \tag{7.3}
\]

Only when the peak reverse current reaches its maximum does a device begin to support voltage. This is the point where the minority carriers on either side of the junction reach zero and the depletion layer widens as carriers are consumed. D1 has the lower recovery charge hence recovers first and supports a reverse bias voltage. D2 recovers subsequently depending on the D1:

- Tail charge;
- Overcharging of the depletion layer; and
- Leakage current.

and natural recombination in the n’ base of D2.

![Dynamic Voltage Sharing](image)

Figure 7.3: Imbalanced voltage sharing of two series connected FWDs
7.3 Snappy Recovery and Imbalanced Voltage Sharing of Two Similar Series Connected FWDs

Dynamic voltage imbalance of series connected diodes is due to their different reverse recovery charges. Two fast recovery power diodes (IXYS: DSEI 8) as in figure 7.4 are used to illustrate the imbalance voltage seen during the reverse recovery period shown in figure 7.5. Hard-switching gate drives ($R_g = 5\Omega$, $V_{ge} = +15V$) are used to drive the series connected IGBTs.

![Diagram of DC chopper circuit](image)

Figure 7.4: DC chopper circuit, $V_s = 150V_{dc}$

(1:20 attenuated voltage differential probe and 1:10 attenuated current probe)

![Waveforms](image)

(a) 25ns (b) 250\mu s

Figure 7.5: Imbalanced voltage sharing with two similar series connected FWDs

($dI_R/dt = 200A/\mu s$, $I_R = 0.84A$)
Both diodes demonstrate snappy recovery, which causes voltage and current oscillations during the reverse recovery process as seen in figure 7.5a. Although both diodes are of the same type, the reverse recovery time of D2 is shorter than the series counterpart, D1. This results in D2 supporting a disproportionate part of the supply voltage, $V_R$, during the reverse recovery process. The different sharing voltages, $\Delta V_R$ in figure 7.5b, after the reverse recovery period are due to the absence of a static resistive network across each diode. As such, the final blocking voltage across each diode is dependent on the individual reverse leakage characteristics [7.9]. Figure 7.5a shows that there are two inter-related manifestations of diode recovery. The first is the voltage oscillation while the second is the peak overshoot voltage at the start of the oscillation.

### 7.4 Suppressing FWD Voltage Oscillation during Reverse Recovery

From equations 7.1 and 7.2, $dI_R/dt$ during the reverse recovery process contributes to diode snappy recovery. If the current turn-on rate of the IGBTs that are commutating the load current can be controlled, the oscillation during FWD reverse recovery can be affected, possibly controlled. The types of IGBTs and anti-parallel diodes used in the experiments are listed in Table 7.1 and subsequent addressing of an IGBT is based on the applicable manufacturers name.

#### Table 7.1: Manufacturer references for the IGBT modules

<table>
<thead>
<tr>
<th>IGBT Code</th>
<th>Current Rating (A)</th>
<th>Voltage Rating (V)</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSM50GAL120DN2</td>
<td>50</td>
<td>1200</td>
<td>Siemens</td>
</tr>
<tr>
<td>GP200MHS12</td>
<td>200</td>
<td>1200</td>
<td>Dynex</td>
</tr>
<tr>
<td>GP600DHB16S</td>
<td>600</td>
<td>1600</td>
<td>Mitel</td>
</tr>
</tbody>
</table>

#### 7.4.1 Suppressing FWD voltage oscillation using a hard-switching gate drive

The devices used in figure 7.6 are Mitel IGBTs with static voltage sharing resistors. The results in figure 7.7 illustrate FWD voltage oscillation suppression through increasing the turn-on time of the commutating IGBT by increasing the gate resistance from 5Ω to 50Ω in the hard-switching gate drive.
Figure 7.6: Half-bridge circuit with hard-switching IGBT, S1 ($V_s = 200$Vdc, $I_L = 1$A)

(a) Voltage turn-on time of 500ns  
($R_g = 5\Omega$, $V_{ge} = +15$V)  

(b) Voltage turn-on time of 1µs  
($R_g = 50\Omega$, $V_{ge} = +15$V)

Figure 7.7: Suppression of FWD voltage oscillation by decreasing IGBT turn-on rate

When the gate resistance is too low to cause suppression of the FWD voltage oscillation, the oscillating effect is injected into the gate of S1 during the Miller discharging period. False turn-off of S1 can occur when the inductive voltage spike due to snappy recovery becomes significantly large as seen in figure 7.7a. By slowing the turn-on of S1 to 1µs, the voltage oscillation is damped and the gate voltage is relatively constant in the Miller discharging region. Adversely, increased gate resistance increases switching delays and switching times, consequently switching losses are increased.
7.4.2 Variation of IGBT turn-on rate using AVC

The AVC technique presented in [7.1] achieves voltage sharing by forcing the IGBT collector voltage to follow a predefined reference during turn-on and turn-off transitions. As a result, $dV_{ce}/dt$ is defined. By introducing a pre-conditioning step to the falling edge of the reference signal, $V_{ref}$, as shown in figure 7.8, tracking control is possible, with the IGBT turn-on $V_{ce}$ (scaled) closely following $V_{ref}$. In order to suppress the diode voltage oscillation, the $dV_{ce}/dt$ at IGBT turn-on has to be reduced. This is possible by decreasing the $V_{ref}$ fall rate. The four parts of figure 7.9 illustrate $V_{ce}$ tracking control using AVC [7.1] with four different turn-on rates. A Mitel IGBT is used for S1 in figure 7.8 and D1 is the internal diode in the Siemens package.

Tracking of the different turn-on rates illustrates the control effectiveness and flexibility of the AVC technique. The minimum turn-on tracking time with AVC is limited to $2\mu s$ for the Mitel IGBT which has a minimum voltage fall-time of about 500ns when hard driven ($R_g = 5\Omega$). The extended $2\mu s$ fall-time is due to the fact that the average load current is only 1A, whence the reverse recovery current is less than 500mA. Hence the fall-time is limited by the free-wheel diode recovery charge. The voltage oscillation that appears before the fall in $V_{ce}$ is due to the voltage overshoot induced by reverse recovery of the free-wheel diode. The voltage overshoot is reflected onto $V_{ce}$ when the AVC is in the pre-conditioning stage, thus initiating the free-wheel diode reverse recovery process. The voltage oscillation will reduce $\alpha V_{ce}$ and causes a slight drop in $V_{ge}$ during the initial turn-on Miller effect period. Large voltage overshoot can temporary turn-off the IGBT and affect AVC operation. In series connection, the FWD voltage overshoot is distributed between the power devices. This minimises the effect of the reflected voltage overshoot.

![Figure 7.8: Pre-condition step in the falling edge of $V_{ref}$](image)
Figure 7.9: Tracking of $V_{ce}$ to $V_{ref}$ with different turn-on transition times

i) **AVC turn-on rates at higher load current**

The fastest fall-time achievable for the Mitel IGBT in figure 7.9 is 2µs. As the free-wheel diode recovery current is small, this limits the IGBT voltage fall-time at turn-on and affects the performance of the AVC circuit. An experiment is conducted using the circuitry in figure 7.10 to shows how fall-time varies when the average load current is increased.
Figure 7.11a shows loss of the AVC tracking when the commutating load current is 0A for a 800ns $V_{\text{ref}}$ fall-time. Figure 7.11b shows proper AVC tracking at 800ns when the load current at turn-on is approximately 12A. Thus, IGBT $V_{\text{ce}}$ tracking at turn-on is dependent on the FWD recovery charge.

Figure 7.10: $V_{\text{ref}}$ tracking when the load current is increased ($R_L = 6\Omega$ or 100\Omega)

7.4.3 Suppressing FWD voltage oscillation with AVC

With the potential of controlling the IGBT turn-on voltage fall rate, AVC is applied to the upper IGBT, S1, and its anti-parallel diode (Mitel) shown in figure 7.6. The results in
parts (a) to (c) of figure 7.12 show typical hard-switching and AVC performance when driving IGBT S1 with $R_g = 22\Omega$ and $R_g = 50\Omega$.

(a) S1 hard-switching ($R_g = 22\Omega$)

(b) S1 hard switched ($R_g = 50\Omega$)

(c) AVC switching of S1 ($R_g = 22\Omega$)

Figure 7.12: Suppressing FWD voltage oscillations

From the results in figure 7.12, the minimum voltage fall-time to eliminate diode reverse recovery oscillation is just less than 1μs. This is achieved with $R_g = 50\Omega$ with the hard gate drive. The AVC technique is able to achieve suppression with a tracking rate of 2μs and $R_g = 22\Omega$. Thus, the AVC technique will be beneficial in high-power applications
where higher load current is required and the turn-on rate can be varied to suppress FWD oscillation.

### 7.5 Active Clamping of FWD Overshoot Voltage during Reverse Recovery

The AVC technique in [7.1] not only allows control of the dynamic $dV_{ce}/dt$ during turn-on and turn-off, it also enables active clamping of the IGBT when its anti-parallel diode reaches a pre-determine voltage ($V_{ref}$) during commutation. During reverse recovery of the diode, its anti-parallel IGBT is in the off-state as a result of underlap. As the diode reverse voltage starts to increase, a small portion of the reverse voltage $V_R$ is fed back to the active gate drive circuit. Hence, when $V_R$ exceeds $V_{ref}$ ($V_{ref} < \alpha V_s$), the IGBT turns on and then turns off once $V_R$ falls back to $V_{ref}$. This action corresponds to actively clamping of the overshoot voltage and transferring the supported voltage energy to a series counter-part. Figure 7.13 illustrates the concept of the active gate drive responding to an overshoot voltage during anti-parallel diode reverse recovery.

![Figure 7.13: The active gate drive circuit responding to FWD voltage overshoot](image)

#### 7.5.1 Determination of AVC response time

The response time of the active gate drive circuit during active clamping depends on the gate resistance, $R_g$, and the IGBT input capacitances, $C_{iss}$. In the AVC process, $V_{out}$ is a
step input because of a rapid rise in the feedback voltage. The gate-emitter voltage, $V_{ge}$, will rise according to the time constant of $R_g$ and $C_{iss}$ as shown in figure 7.14.

$$V_{ge} = V_{out} \left[ 1 - e^{-\frac{t}{R_g C_{iss}}} \right]$$

**Figure 7.14: Simplified concept for the response time of active clamping**

AVC response time for the active clamping of $V_R$ is determined by the gate turn-on delay time, $t_{d(on)}$. $V_R$ starts to be actively clamped when $V_{ge}$ reaches the IGBT turn-on threshold voltage, $V_{ge(th)}$. A faster response is preferable but this requires either $R_g$ and/or $C_{iss}$ to be smaller. $C_{iss}$ is device dependent. Reducing $R_g$, however, will pose stability problems for the control system as the dominant complex poles will lie in the right region of the root locus plot [7.21, pp. 82].

**i) The minimum reverse overshoot voltage for active clamping**

The level of $\ddot{V}_R$ for the AVC to clamp the overshoot, depends on $V_{out}$ which should be equal to or greater than $V_{ge(th)}$. This will ensure that $V_{ge}$ is sufficient to turn-on the IGBT. Once $V_R$, whence $V_{out}$ is less than $V_{ge(th)}$, the IGBT will turn-off. The rate of rise and fall of $V_{ge}$ will depend on the time constant of $R_g$ and $C_{iss}$. Figure 7.15 illustrates the rise and fall of $V_{ge}$ with respect to $V_R$ and $V_{out}$.

In period I, the FWD is in a forward biased condition. The negative voltage drop across the IGBT is the diode forward voltage. Once the diode has reached the peak reverse recovery current (period II), the voltage across the diode (and IGBT) rises. This voltage rise is fed back to the active gate drive and into the differential amplifier, producing a proportional output voltage to the gate terminal (period III). The gate voltage rate of rise will be determined by the time constant of the gate resistance and IGBT input capacitance.
(which is voltage dependent). On reaching the turn-on threshold voltage, the IGBT turns on and the overshoot voltage is actively clamped (period IV).

![Diagram showing voltage control and compensation network](image)

Figure 7.15: Basic concept of $V_{ge}$ control with respect to $V_R$ and $V_{out}$

### 7.5.2 Compensation of the voltage detection network

Accurate closed loop AVC depends on the IGBT voltage detection network, which consists of a resistive voltage divider across an IGBT as shown in figure 7.16. The scaled down collector voltage during the transition-states is fed to the differential amplifier and compared with the pre-determined reference signal. In order to ensure that the transient response of the fed back collector voltage signal tracks the actual IGBT collector voltage, the voltage detection network has to be tuned. The role of the capacitor $C_s$ is to ensure the two time constants shown in figure 7.16 are the same, thereby ensuring the voltage output is critically damped with respect to the collector voltage. Figure 7.17 shows the voltage transient response of each resistor with respect to the collector voltage.
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Voltage Detection Network

Compensating Capacitor

Only If Necessary

Note: C1 and C2 are resistance parasitic capacitances.

Figure 7.16: Diagram of the voltage detection circuit

 transient response is well-matched

Figure 7.17: Transient response of the voltage detection network \( (V_s = 100V_{dc}) \)

With \( V_s = 100V_{dc} \), the voltage response from the resistor divider follows the collector voltage. Since the voltages across R1 and R2 match \( V_c \), no compensating capacitor is required to tune the voltage detection network. Such compensation is usually required when higher voltages are measured, and the two resistors have very different constructions because of the high resistance and voltage rating of R1.
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7.6 Active Clamping of Two or More Series Connected FWDs

7.6.1 Simulation of two series connected FWDs

Simulation using Orcad PSpice can analyse the control theory with two series connected IGBTs with their anti-parallel diodes each blocking 100Vdc, in a half bridge circuit. The PSpice parameter values in the active gate drive are shown in Table 7.2:

In figure 7.18, the two ambipolar recombination lifetimes of the FWDs are different in order to create an unbalanced voltage sharing condition during reverse recovery. The simulation result in figure 7.18a is based on having the minimum reverse overshoot voltage that will activate the AVC. Once $V_{out}$ is higher than the IGBT gate threshold, the overshoot voltage $V_R$ will fall exponentially depending on the rising rate of the series counterpart, $D_{2L}$. Once the overshoot approaches the $V_R$ that produces a $V_{out}$ lower than $V_{ge(th)}$, the IGBT turns off and active clamping action stops. The voltage supported by the IGBT will depend on the other series connected devices. In this simulation, active clamping starts at 20% above the theoretical sharing voltage level. The delay time for $V_{ge}$ to reach the IGBT turn-on threshold depends on gate resistance, IGBT input capacitances, and $V_{out}$.

The simulation result in figure 7.18b illustrates a higher $V_R$ condition which produces a larger $V_{out}$. With a higher $V_{out}$, the response time is reduced due to an increase in the gate current charging up the input capacitance and the gate voltage eventually falls at a slower rate. This allows the voltages to converge in figure 7.18b before the gate voltage falls below the turn-on threshold voltage. The clamped voltage supported by both devices after the commutating process is dependent on the static resistive network and in this simulation, both devices support half the supply voltage.

Figure 7.18c shows graphically the effect of different $V_R$ levels on AVC response time. As the overshoot voltage, $\Delta V_R$, increases, the response time for active clamping reduces. This corresponds to an increase in the rate of rise of the recovery voltage, $dV_R/dt$. A limit will be reached where any further increase in $dV_R/dt$ will not reduce the response time as the output voltage from the differential amplifier, $V_{out}$, is saturated. $dV_R/dt$ is dependent on the recovery time difference of the series FWDs, which dominates AVC response time.
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(a) Minimum level of $V_R$ for active clamping

(b) High level of $V_R$ for active clamping

(c) Effect of $V_R$ level on AVC response time

Figure 7.18: PSpice results illustrating active clamping and its response time
Table 7.2: PSpice parameter values for the active gate drive simulations

<table>
<thead>
<tr>
<th>Active Gate Drive Parameters</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{ref}}$</td>
<td>11</td>
<td>V</td>
</tr>
<tr>
<td>$\alpha V_R$</td>
<td>7.9</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{ge(th)}}$</td>
<td>5.45</td>
<td>V</td>
</tr>
<tr>
<td>G</td>
<td>3.5</td>
<td></td>
</tr>
<tr>
<td>$R_G$</td>
<td>22</td>
<td>Ω</td>
</tr>
<tr>
<td>$C_{\text{iss}}$</td>
<td>140</td>
<td>nF</td>
</tr>
</tbody>
</table>

### 7.6.2 Active clamping of two series connected FWDs

The test circuit in figure 7.19 is used to practically evaluate active clamping of two series FWDs. Figure 7.20a illustrates two similar IGBTs (S1, S2L, and S2U - Mitel) and figure 7.20b illustrates two different IGBTs (S1, S2L - Mitel and S2U - Dynex) with and without AVC. Note that by Kirchhoff’s voltage law, AVC is not needed for one switch/diode, provided the supply is decoupled.

![Figure 7.19: Half-bridge circuit with AVC applied to IGBTs S1 and S2U](image)

$(V_s = 200Vdc, \bar{I}_L = 1A)$
The gate voltage of $S_{2U}$ must be at its turn-on threshold voltage in order to actively clamp the overshoot voltage. Once $S_{2U}$ is on, its supported voltage is reduced and the extra voltage is transferred to the series counter-part. The voltage fall rate for $S_{2U}$ will depend on the voltage rise of $S_{2L}$. The voltage sustained on the uncontrolled FWD clearly indicates the unbalance sharing during reverse recovery. The voltage imbalance is gradually reduced as the static resistor network balances FWD steady-state voltage. With AVC, the voltage difference $\Delta V$, is reduced and the FWDs quickly support equal voltages.
7.6.3 **Active clamping of three series connected FWDs**

Three series connected IGBTs using two different diode types are shown in figure 7.21 (S1, B3 - Mitel and B1, B2 - Dynex), where each blocks 100Vdc in the off-state. IGBT S1 is hard switched but with a 50Ω gate resistance to suppress any voltage oscillation (refer to figure 7.12b). The result with active clamping is shown in figure 7.22a.

As shown in figure 7.22b, without external control the bulk of the reverse voltage is shared between B1 and B2. In this experiment, diodes B1 and B2 have a faster recovery time than B3. The commencement of AVC is observed on B1 and B2 at $V_s = 250Vdc$ (figure 7.22c). Once clamped at this voltage level, AVC does not turn-on the IGBTs again. However at a higher voltage level ($V_s = 300Vdc$), the active clamping effect observed in figure 7.22d is due to the significant difference in reverse recovery times of the three series connected FWDs. Once the AVC clamps B2, B1 supports the extra voltage and B2 voltage drops as B1 voltage increases. However, this causes B1 to be actively clamped and the extra voltage is returned to B2, which results in repeated AVC action. This process continues until B3 recovers and its voltage rises. The current and voltage independence of AVC makes this technique applicable to high-power.

![Figure 7.21: Half-bridge circuit with AVC technique](image)

$(V_s = 300Vdc, \dot{I}_L = 3A)$
Chapter Seven: AVC of Series Connected FWDs

(a) Active clamping on three series connected FWDs

(b) Imbalanced voltage sharing of three series connected FWDs

(c) Active clamping for under voltage conditions ($V_s = 250\text{Vdc}$)

(d) Active clamping on three series connected FWDs ($V_s = 300\text{Vdc}$)

Figure 7.22: Active clamping on three series connected FWDs with a 3A load current
7.7 Active Voltage Clamping Incorporating a Passive Snubber
AVC is effective in controlling diode recovery voltage oscillations but may not be fast enough to control the initial voltage overshoot at diode recovery.

7.7.1 Active clamping of FWD voltage overshoot when utilising a passive snubber
Typical FWD reverse recovery is in the range on hundreds of nanoseconds for fast-recovery high-power diodes. The response time for the AVC to react to an overshoot voltage during reverse recovery depends on the time constant of the gate resistance and IGBT input capacitances. Slow-recovery diodes are not suitable for high-speed applications, since they reduce the efficiency of high-power inverters. Thus, the main limitation of AVC is the initial delayed response time. This can be seen in figure 7.20 where some imbalance persists. An alternate method to clamp diode initial voltage overshoot is to utilise a passive snubber circuit in conjunction with the AVC technique, whereby the initial fast transient overshoot voltage can be minimised. Figure 7.23 shows the common types of passive turn-off snubbers, which include a simple C, an RC, and an RCD configuration.

![Figure 7.23: Common passive turn-off snubber configurations](image)

The snubber in figure 7.23a is best for slowing and reducing the \( \frac{dV_{ce}}{dt} \) but the IGBT will tend to suffer higher current stress during turn-on \( [i = \frac{dV}{dt}] \). The addition of the snubber series resistor \( R \) in figure 7.23b limits the charging and discharging capacitor current and dissipates the capacitor energy at reset. However, if the snubber time constant is less than the IGBT voltage fall-time \( (RC < t_f) \), at turn-on the capacitor energy is
dissipated in the IGBT. Figure 7.23c allows the full capacitor snubber effect at turn-off and diode recovery through the diode charging path and controls current at turn-on via the snubber resistor. Although this configuration inherits the advantages of both the C and RC snubbers, its component count is higher and results in a complex, costly structure at high voltages. The best snubber compromise is that in figure 7.23a. The IGBT turn-on current limitation when using a simple C snubber is minimised by the AVC technique, as dV_{ce}/dt at turn-on is well defined. This limits the capacitor discharge current and its presence results in a net increase in device loss at turn-on [1/2CV^2]. The only significant difference will occur during the pre-conditioned step period. As dV_{ce}/dt is zero once this step is reached, the effect is small.

The various snubber circuits are assessed using the circuit in figure 7.24. Figure 7.25 compares the switching losses of an active controlled IGBT (S1 - Mitel) with and without the snubber circuit. Although turn-on losses are slightly increased, the turn-off losses are slightly decreased. Figure 7.26 shows the snubber capacitor current during the switching transitions for an RC and C snubber.

![Figure 7.24: DC chopper circuit with a single IGBT under AVC operation](image)

(V_s = 200Vdc, \bar{I}_L = 1A, D1 - Siemens internal diode)
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Figure 7.25: Comparison of switching losses for AVC with and without RC or C snubbers

From the results shown in figures 7.25 and 7.26, the IGBT switching losses and current stresses at turn-on are not significantly different for the unaided or RC/C snubber cases with AVC switching. The main difference is during the pre-conditioned step. With $\pm dv_{ce}/dt$ fully controlled, the snubber resistor can be omitted, which results in a simpler snubber circuit. The snubber capacitance that is required with AVC must satisfy two conditions:

- Able to clamp the initial overshoot voltage to a specific level and
- Not affect AVC operation of the series connected IGBTs.
The snubber capacitance required to clamp the initial overshoot voltage depends on the specified overshoot voltage percentage and the number of series devices for a fixed operating voltage source. In the case where the snubber capacitance is larger than the junction capacitance of the diode (and parallel IGBT) during reverse recovery, the snubber capacitance $C_s$ can be determined by:

$$C_s = \frac{\Delta Q}{\Delta V}$$

where $\Delta V$ = FWDs transient voltage sharing differences

$\Delta Q$ = difference in reverse recovery charge of the series connected FWDs

The capacitance in Chapter 3.1.2 gives the worst case requirement, which is in excess of the needs to only control the initial voltage overshoot magnitude.

### 7.7.2 Active clamping of two series connected FWDs with snubber capacitance

Two experiments, one with S1, S2L and S2U - Mitel and the other with S1 and S2L - Mitel and S2U - Dynex, are performed with the snubber circuit in figure 7.27. The results in figures 7.28 and 7.29 illustrate the initial transient overshoot voltage being clamped to a...
maximum of 30% more than the ideal steady-state balance voltage. An external snubber $C_s$ is connected across the FWD to create imbalanced voltage sharing.

Figure 7.27: Half-bridge circuit with AVC utilising a snubber circuit

(V$_s$ = 200Vdc, I$_L$ = 1A)

Figure 7.28: Comparison of AVC performance with and without C snubber for two similar IGBTs
The addition of the snubber eliminates the initial transient overshoot. This reduces IGBT voltage stress and allows the device to be used with a supply closer to its voltage rating. The capacitance in the experiments is based on equation (7.4) to minimise the transient overshoot. AVC is effective and minimises the voltage imbalance.

### 7.7.3 Comparison of FWD voltage sharing between AVC plus snubber and uncontrolled passive snubber

With referenced to figure 7.27, two different IGBTs (S1 and S2L - Mitel and S2U - Dynex) are used to compare FWD voltage sharing under active clamping and uncontrolled hard-switching, both with a passive snubber. Although FWD recovery transient voltage balancing can be achieved with a snubber, this is not preferred with AVC as the required large snubber capacitance dominates IGBT switching performance.

In figure 7.30, 2nF capacitance is used with both switching techniques. The objective is to clamp only the initial transient overshoot and determine the voltage droop for S2U. Although both techniques achieve voltage sharing in about the same time, the voltage difference, $\Delta V$, is smaller with AVC. The increased voltage rise of S2L is a result of the active clamping of S2U, whereas in the uncontrolled case, the voltage of S2L is dominated by the static resistor network.
7.7.4 Low current transient voltage balancing of series connected IGBTs with snubbers

For series connected, controlled IGBTs with a C snubber, the charging current available to the snubber capacitance and device capacitances during the turn-off transition must be sufficient to maintain $dV_{ce}/dt$ tracking. As such, the load current must not be lower than the required charging current for the specified $dV_{ce}/dt$ rate [$i = C_dV/dt$]. In the case of sinusoidal PWM inverter operation, the load current will fall to zero which will affect turn-off control of the series IGBTs. Although this will cause the IGBT $dV_{ce}/dt$ to be dominated by the snubber capacitance, transient voltage sharing will be enforced by the snubber and the static resistive networks. But capacitor tolerance may be ±20%, therefore the capacitances should be matched to within 1%. Figure 7.32 illustrates transient voltage balancing of two series connected IGBTs (S1, S2L, and S2U - Mitel) during turn-off with C snubbers.
AVC tracking is lost once the snubber dominates IGBT voltage rise at turn-off. Any difference in transient voltage sharing will be determined by the snubber capacitance tolerance, and small capacitance is preferable to minimise voltage differences. The results shown in figure 7.32b indicate that dynamic voltage sharing occurs at low load current.
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7.8 Summary

i) Voltage oscillation
The effects of using the AVC technique to suppress FWD voltage oscillation have been demonstrated. As the IGBT turn-on rate is decreased, the amplitude of the overvoltage oscillation is reduced. The features of this technique for controlling diode recovery voltage oscillations are summarised in Table 7.3.

Table 7.3: Features of utilising AVC for suppressing FWD oscillation

<table>
<thead>
<tr>
<th>Advantages:</th>
<th>Disadvantage:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prevents snappy recovery effect</td>
<td>Increases IGBT turn-on and turn-off losses</td>
</tr>
<tr>
<td>Control of FWD voltage oscillations</td>
<td></td>
</tr>
</tbody>
</table>

ii) Voltage overshoot
Active clamping of FWD overshoot voltage is effectively demonstrated using AVC, where the FWD voltages eventually balance. When one of the FWDs is actively clamped, its supported voltage is reduced and excess voltage is transfer to a series counter-part. The slower recovering FWDs will thereby support the transferred voltage and this results in balanced voltage sharing among the FWDs. The features of this clamping technique are summarised in Table 7.4.

Table 7.4: Features of utilising AVC for FWD active voltage clamping

<table>
<thead>
<tr>
<th>Advantages:</th>
<th>Disadvantage:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prevents overshoot voltage from damaging devices</td>
<td>The overshoot voltage threshold before AVC activation, is determined by the active gate drive circuit parameters</td>
</tr>
<tr>
<td>Active voltage sharing through clamping the overshoot voltage</td>
<td></td>
</tr>
</tbody>
</table>

The overshoot voltage threshold which activates AVC is determined by the differential amplifier gain, the maximum level of $V_{\text{ref}}$, the feedback ratio from the static resistor network, and the gate resistance. These four parameters are crucial for AVC stability [7.21, pp. 73] and some of these parameters vary with different IGBTs. In the experiments conducted, the threshold is nominally 150% of the specified blocking voltage (100Vdc). As such, the IGBT has to be rated at 1.5 times the pre-determined blocking voltage in high-power applications.
iii) Capacitance snubber

The initial transient overshoot voltage seen with active clamping may result in a short period, high-voltage stress seen by the anti-parallel diode (hence IGBT) that has the shortest recovery time. This initial transient peak can be minimised by utilising a C snubber across each FWD. As IGBT $\pm dV_c/dt$ is controlled, the snubber capacitance will not impose a high current stress on the IGBT during the turn-on transition. The necessary capacitance could be calculated to eliminate the transient peak and AVC assumes active clamping after the response delay. This allows smaller snubber capacitance.

An advantage of a turn-off snubber is that IGBT turn-off switching loss is reduced. Although the stored energy in the snubber capacitor is dissipated in the IGBT during the turn-on transient, the total IGBT losses (turn-on plus turn-off) can be lower than those for the unaided case, if the capacitance is sized properly [7.23, pp. 160]. Figure 7.33 illustrates the theoretical IGBT loss components when using a C snubber with the assumption that the collector current falls according to $i_c = I_m(1 - t/t_i)$. The turn-on loss is increased by $\frac{1}{2}CV^2$ and the current stress at turn-on is controlled by the AVC tracking.

The IGBT total loss, $W_T$, can be described by the following equations [7.23, pp.160]:

- If the capacitor charges fully before the collector current has reached zero, $k \leq 1$, $W_T$ can be described by:
  \[
  W_T = \frac{V_s I_m t_{fi}}{2} \left(1 - \frac{4k}{3} + k^2 \right) \quad (J) \quad (7.5)
  \]

- If the capacitor does not charge fully before the collector current reaches zero, $k \geq 1$, $W_T$ is described by:
  \[
  W_T = \frac{V_s I_m t_{fi}}{2} \left(\frac{k^2 - k + \frac{1}{4}}{k - \frac{1}{2}} \right) \quad (J) \quad (7.6)
  \]

The snubber capacitor, $C$, is determined by [7.23, pp.160]:

- For $k \leq 1$
  \[
  C = \frac{I_m t_{fi}}{V_s} \left(\frac{1}{2}k^2 \right) \quad (F) \quad (7.7)
  \]

- For $k \geq 1$
  \[
  C = \frac{I_m t_{fi}}{V_s} \left(k - \frac{1}{2} \right) \quad (F) \quad (7.8)
  \]
When \( k \leq 1.4 \), theoretically the total losses are less than those for an unaided IGBT. At \( k = \frac{1}{3} \), where the IGBT turn-off loss is equal to the IGBT extra turn-on loss, the minimum total loss condition exists. To achieve this condition, the snubber capacitance may be small \([C = 2I_{m}t_{f}/9V_{s}]\). This is desirable in AVC switching, as the snubber requirement is only to eliminate the initial transient voltage overshoot. The snubber capacitance will dominate the turn-off \( dV_{cc}/dt \) at low load current. AVC tracking during this period may be lost for the series connected IGBTs. Voltage balancing will be dominated by the snubber capacitance and the static sharing resistors. The features of adding a C snubber are given in Table 7.5.

![Figure 7.33: Loss components for a transistor aided by a capacitance-type snubber](7.23, pp.161)
Table 7.5: Features of utilising AVC with a snubber

<table>
<thead>
<tr>
<th>Advantages:</th>
<th>Disadvantages:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Minimises initial transient overshoot at IGBT turn-off or diode reverse recovery</td>
<td>• Additional passive component.</td>
</tr>
<tr>
<td>• Reduces IGBT turn-off losses and diode reverse recovery losses</td>
<td>• Possible loss of controlled turn-off dV_{ce}/dt tracking with low load current.</td>
</tr>
<tr>
<td>• Improves dV_{ce}/dt turn-on tracking at low currents due to capacitor discharge current</td>
<td>• Additional IGBT turn-on losses (\frac{1}{2}CV^2)</td>
</tr>
<tr>
<td></td>
<td>• Capacitances must be matched</td>
</tr>
</tbody>
</table>

**iv) Conclusion**

The AVC results indicate a response delay in clamping the overshoot voltage. This delay is due to the process of desaturating the differential amplifier output [7.22] and the IGBT gate charging time. This response delay can be minimised with a higher differential gain and lower gate resistance but these factors may cause AVC instability [7.21, pp. 73].

For AVC to be employed in high-voltage inverter applications, FWD reverse voltage balancing and fault prevention have to be considered. This chapter illustrated an AVC technique that performs the dual roles of suppressing the voltage oscillation produced by snappy recovery and actively clamping of the associated overshoot voltage. If the AVC response time is insufficient to clamp the voltage associated with the initial diode recovery snappy, snubber capacitance may be added. AVC will ensure that capacitor discharge is well controlled. The net device turn-on loss is increased but overall losses are decreased. The effectiveness of the AVC technique can be summarised as:

- Allows dynamic voltage balancing of series connected FWDs and IGBTs;
- Snubber circuits are not needed to achieve dynamic voltage balancing, unless compromise is required to minimise the FWD initial peak voltage overshoot;
- Elimination of failures due to FWD reverse recovery overvoltage;
- The active gate drive serves the dual purposes of controlling both IGBT operation and their anti-parallel diodes in inverter applications; and
- Discharge of parallel connected snubbers is controlled.

Figure 7.34 encapsulates the design issues associated with series connection of IGBTs and anti-parallel diodes, in high-voltage inverter designs. In particular, the FWD voltage
failure conditions due to snappy recovery are highlighted and the methodologies to avoid failure are stated.

Figure 7.34: Overview of design issues associated with series connected FWDs
References


CHAPTER EIGHT

Conclusion

The use of a power semiconductor device for high-power application depends on its reliability, electrical ratings, and associated operating circuitry. A comparison between the IGCT and the IGBT, for medium to high voltage applications, was presented in Chapter 1 (Table 1.4). The safe operating area and switching characteristics of the IGBT allow its use in a wide range of circuit techniques. At present, IGBTs are limited by a maximum voltage rating of 6.5kV, module dissipation, and current ratings [8.1]. Ongoing research to enhance voltage, current, and thermal handling capabilities has been extensively reported in the literature (see Chapter 1). Utilising currently available IGBTs in medium to high voltage (≥11kV) designs requires some form of series connection. The different methodologies considered in Chapter 2 (figure 2.11) include:

- Multi-level converters and
- Series connected power devices.

Direct series connected IGBTs for medium voltage drives (2.3kV-6.9kV) has been the focus of recent research and the different topologies involved are presented in Chapter 3 (figure 3.18). Two design issues related to series connection are static and dynamic voltage sharing. Conventional techniques for achieving balanced voltage for each stage were described in Chapter 3.1, and utilise

- a resistive network for static voltage balancing and
- a capacitive network for dynamic voltage sharing.

Using a resistive network for static voltage control reduces circuit design complexity and is effective. However, resorting to a capacitive network for dynamic voltage control may result in high total switching losses and increased equipment size. Different dynamic voltage control techniques were described in Chapter 3 (Table 3.1) and are classified as:

- Load side control and
- Gate side control.

Load side control depends on passive high power components, which incurs the same limitations as a capacitive network. The desire to fully control IGBT switching characteristics has lead to several control techniques (gate side control) which eliminate the passive components but increase circuit design complexity. Apart from control of
IGBT dynamic voltage sharing, enhanced switching performance and fault protection are additional aspects that can be gained with gate side control (Chapter 4).

Gate side control of series connected IGBTs depends on either synchronous switching or precise gate current modulation to balance the dynamic collector voltages. In this thesis, the use of active gate control with IGBT collector-emitter voltage feedback to achieve active voltage control (AVC), has been investigated.

The AVC described in reference [8.2], with additional enhanced control features for the pre-condition step period and $dV_{ce}/dt$ variation, was considered in Chapter 5. The technique is based on the IGBT collector voltage tracking a pre-determined reference signal, $V_{ref}$. A digital, rather than analogue approach, is used to generate the $V_{ref}$. Digital methods allow controllability and flexibility for varying IGBT $dV_{ce}/dt$ and minimising switching losses. The features of both circuit approaches were described in Chapter 5.5.

Experimental results for two and three series connected IGBTs were presented in Chapter 6. Three different IGBT modules (Siemens – 1.2kV/75A, Dynex – 1.2kV/200A, and Mitel – 1.6kV/600A) were used to demonstrate AVC effectiveness at supply voltages of 300Vdc or less. The research presented concentrated on increased AVC functionality and its extension to bridge leg applications. To increase reliability, repeatability, and flexibility, these features were investigated at reduced voltage and current. The functions demonstrated included:

- Adaptive control of the pre-conditioning step;
- $dV_{ce}/dt$ variation;
- Load current and device case temperature variation; and
- IGBT tail current effects.

In medium-voltage inverters, the series connected IGBT anti-parallel diodes provide the free-wheeling path during commutation. The difference in diode reverse recovery characteristics results in imbalanced dynamic voltage sharing. The ability of AVC to actively clamp voltage overshoot and suppress voltage oscillations due to diode snap recovery was demonstrated in Chapter 7. The dual role of AVC controlling dynamic voltage sharing for both series connected IGBTs and free-wheel diodes enhances the potential of integrating AVC into medium-voltage drives.

Figure 8.1 summarises the experiments conducted using the proposed AVC approach.
Figure 8.1: Summary of the AVC experiments conducted

The main advantage of gate side control for IGBT series operation is the elimination of the large passive components used to achieve dynamic voltage sharing. However a low snubber capacitance across each IGBT, with the presented AVC technique, allows dynamic voltage sharing at low load current. It also minimises the initial transient voltage overshoot at IGBT turn-off and at diode reverse recovery. Table 8.1 summarises the features of the presented AVC technique applied to series connected IGBTs.

Table 8.1: Feature summary of the presented AVC technique

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
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<tbody>
<tr>
<td>• Redundancy control (voltage redistribution)</td>
<td>• Additional switching losses due to pre-conditioning step</td>
</tr>
<tr>
<td>• Load current and temperature independent</td>
<td>• IGBT dV&lt;sub&gt;ce&lt;/sub&gt;/dt is restricted to the slowest switching device</td>
</tr>
<tr>
<td>• Dual role of dynamic voltage control of series connected IGBTs and FWDs</td>
<td>• Careful PCB layout of the digital circuitry is necessary to avoid electromagnetic interference</td>
</tr>
<tr>
<td>• Clamped the overshoot voltage during IGBT tail current interval</td>
<td>• An initial response time delay is required before the AVC can clamp the overshoot voltage during FWD reverse recovery and the IGBT tail current</td>
</tr>
</tbody>
</table>
Chapter Eight: Conclusion

8.1 Author’s Contribution

A digital approach for the AVC technique described in Chapter 5 has been implemented to control the series operation of IGBTs. The research focused on AVC effectiveness with low voltage analysis and the design factors related to inverter applications. Figure 8.2 summarises the research performed and the focus areas are:

- A digital approach for controlling the $V_{ref}$ rate during AVC operation has been implemented with an FPGA controller. Two AVC features are incorporated to minimise IGBT switching losses and provide system controllability for voltage sharing/redistribution;

- The features of gate side control by gate signal synchronisation [8.3] were illustrated experimentally, with its limitations highlighted and discussed;

- Different IGBT modules were tested with the proposed AVC technique, at low voltages ($\leq 300$Vdc) and variable load current ($\leq 20$A) with two and three series connected devices, in order to determine AVC features applicable to medium and high voltage applications;

- The effect of the IGBT turn-off tail current during series operation has been analysed and the effectiveness of AVC during this period has been established;

- The AVC dual role of balancing dynamic voltage of series connected IGBTs and their anti-parallel diodes has been substantiated for inverter application. This validation includes the effects of a capacitive snubber across the IGBT for low load current and its effectiveness in AVC clamping of FWD overshoot voltage during reverse recovery;

- The prototype AVC gate drive as shown in Appendix A, has been implemented; and

- The high-voltage test system, capable of generating 15kVdc (20kVA), has been constructed as shown in Appendix B.
8.2 Recommendations for Future Research

Future research applicable to enhancing the AVC technique include:

- The next stage in the evaluation of the presented AVC technique for series connected IGBTs, is to progress to a medium-voltage level (2.3kV-6.9kV). Demonstrating the technique at typical medium voltage and current levels will require addressing engineering issues such as electromagnetic interference (EMI), test rig protection, and the voltage ratings of auxiliary passive components;

- The present gate drive incorporates the AVC technique described in Chapter 5. The fault protection capabilities described in Chapter 4.4 need to be incorporated into the gate drive, before any medium to high voltage testing. These proposed features prevent IGBT short-circuit, for at higher voltage conditions, the EMI may cause digital circuitry malfunction during switching;
The turn-off pre-conditioning step period was determined through practical experimentation on specific IGBT modules (see Chapter 5.5i). A mathematical model incorporating IGBT characteristics [8.4] could be developed and evaluated in order to approximate the required step period;

- Previous modelling and characterisation of AVC involved a single IGBT [8.5]. Characterisation should be extended to two and three devices which will allow further AVC understanding during series operation;

- IGBT tail current decay time differences results in imbalanced voltage sharing after the initial dynamic turn-off transient. Although AVC is capable of clamping the overshoot voltage, its respond time causes the IGBT to sustain an initial overshoot voltage, \( \Delta V \). Low static sharing resistance minimises \( \Delta V \) but results in larger component size due to a higher power requirement. A graphical plot illustrating the relationship between \( R_s \), the \( \Delta V \) sustained, and the power dissipation, \( P_D \), by the resistor can be evaluated at a particular operating voltage, as shown in figure 8.3. The tradeoff between \( \Delta V \) and \( P_D \) when selecting \( R_s \), should be analysed; and

- Some form of gain scheduling could be used in the feedback control loop in order to increase the gain at higher collector voltages. This may allow more effective voltage clamping during the tail current interval.

![Figure 8.3: Selection of \( R_s \) at a particular operating voltage](image-url)
Chapter Eight: Conclusion

References


APPENDIX A

Experimental Setup and AVC Gate Drive

A.1 Experimental Setup for Three Series Connected Mitel IGBTs

A.2 Top View of the Global Controller
A.3 Top View of the Local Gate Controller

1. Fibre Optic Communication
2. Auxiliary Switches For External Control
3. Gate Drive Circuit
4. Ramp Circuit
5. $V_{cc}$ Detection Circuit
6. Static Balancing Resistor Network - thick film power resistors
APPENDIX B

Pictorial Views of the High-voltage Test System

B.1 Structural Layout

B.2 Overview of the High-voltage Test System

[1] Three Phase Transformer - 20kVA, 11kV_{rms}, 1.05A_{rms}
[2] Three Phase Inductor - 10mH, 11kV_{rms}, 100A_{rms}
[3] Three Phase Bridge Rectifier - 30kV_{pk}, 727A
[4] Inductive Load - 20mH inductor with anti-parallel free-wheel diodes (11kV, 100A_{rms}, impedance = 6963Ω at 50Hz)
B.2.1 Three Phase Transformer

Transformer specification:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Primary</th>
<th>Secondary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage ((V_{rms}))</td>
<td>415</td>
<td>11,000</td>
</tr>
<tr>
<td>Ampere ((A_{rms}))</td>
<td>27.8</td>
<td>1.05</td>
</tr>
<tr>
<td>Reference Power ((VA))</td>
<td></td>
<td>20,000</td>
</tr>
<tr>
<td>Frequency ((Hz))</td>
<td></td>
<td>50</td>
</tr>
</tbody>
</table>

B.2.2 Three Phase Inductor \((10mH/phase)\)

Inductor specification:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Rating</th>
</tr>
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<tbody>
<tr>
<td>Voltage ((V_{rms}))</td>
<td>11,000</td>
</tr>
<tr>
<td>Continuous Amperes ((A_{rms}))</td>
<td>100</td>
</tr>
<tr>
<td>Inductance per phase ((mH))</td>
<td>10</td>
</tr>
<tr>
<td>Frequency ((Hz))</td>
<td>50</td>
</tr>
<tr>
<td>Impedance ((\Omega))</td>
<td>3278</td>
</tr>
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</table>
Appendix B. Pictorial View of the High-voltage Test System

B.2.3 Three Phase Bridge Rectifier

[1] Five series connected rectifier diodes, each aided with RC snubber (R = 680Ω at 10W, C = 0.1μF at 3.5kV), using Dynex-DS1112SG

[2] Forty series connected capacitors, $C_{\text{link}}$, using 450Vdc, 470μF aluminium electrolytic type with 47kΩ, 10W balancing resistor in parallel

Rectifier diodes specification:

<table>
<thead>
<tr>
<th>Parameter Rating</th>
<th>Parameter Rating</th>
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<tbody>
<tr>
<td>Total Repetitive Peak Reverse Voltage ($V_{pk}$)</td>
<td>30,000</td>
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<tr>
<td>Maximum Continuous Forward Current (A)</td>
<td>727</td>
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Capacitors link specification, $C_{\text{link}}$:

<table>
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<tr>
<td>Total Capacitance ($\mu$F)</td>
<td>11.75</td>
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<tr>
<td>Total Equivalent Series Resistance (Ω)</td>
<td>7.76</td>
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<tr>
<td>Total DC Voltage (Vdc)</td>
<td>18,000</td>
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<tr>
<td>Maximum Peak to Peak Ripple Current (A)</td>
<td>10</td>
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<tr>
<td>Maximum Peak to Peak Ripple Voltage (V)</td>
<td>68</td>
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</table>
B.2.4 Inductive Load - 20mH inductor with anti-parallel free-wheel diodes

[1] Three phase inductor with 20mH at each phase
[2] Three series connected free-wheel diodes (Powerex-R5021613FSWA), D\textsubscript{FWD}, each aided with RC snubber (R = 9.4Ω at 100W, C = 21.4nF at 2kV).

Inductor specification:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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<tbody>
<tr>
<td>Voltage ($V_{rms}$)</td>
<td>11,000</td>
</tr>
<tr>
<td>Continuous Amperes ($A_{rms}$)</td>
<td>100</td>
</tr>
<tr>
<td>Inductance per phase (mH)</td>
<td>20</td>
</tr>
<tr>
<td>Frequency (Hz)</td>
<td>50</td>
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<tr>
<td>Impedance ($Ω$)</td>
<td>6963</td>
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Free-wheel diodes specification, D\textsubscript{FWD}:

<table>
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<tr>
<td>Total Repetitive Peak Reverse Voltage ($V_{pk}$)</td>
<td>4200</td>
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<tr>
<td>Maximum Continuous Forward Current (A)</td>
<td>125</td>
</tr>
</tbody>
</table>
APPENDIX C

Circuit Diagrams
Appendix C. Circuit Diagrams

CCT TO GENERATE RISE AND FALL EDGE PULSES

CLK2X = 100MHz

CLK = 6.25MHz

EXTERNAL 50MHz CLK I/P TO GENERATE 6.25MHz & 100MHz

Heriot-watt University
EPS-EECE
Edinburgh EH14 4AS
Date Last Modified: 3/16/05

Xilinx: Local Gate Control
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Date: 3/14/05
Appendix C. Circuit Diagrams

U96
State Machine
ADC_START
CO_RISESTEP
CO_RISESTEP TR_EN
FALL_EDGE
FALL_EDGE CONTRISE
RISTEP ADC_END
RISE EDGE
CE
CE_FALLSTEP
CLK
F1
R1
SEL0
SEL1
SEL2
STOP
IV0
IV1
IV2
IV3
IV4
IV5
IV6
IV7
QB0
QB1
QB2
QB3
QB4
QB5
QB6
QB7
SRCLRISESTEP
SCLR_FALLSTEP
CONTR1

U98
COREGen Module
CE
TR_EN
CLK
Q2[0]
IN_SELECT_RATE[2:0]
EXTERNAL_SELECT[2:0]

U97
COREGen Module
DE
MA[2:0]
QB2[0]
Q_SELECT_RATE[2:0]

U99
COREGen Module
QL[2:0]
Q<Select_Rate>[2:0]

SEL[2:0]

IV[7:0]

QB[7:0]
Appendix C - Circuit Diagrams

U100
COREGen Module
CE, CLK, CE
STOP

U101
COREGen Module
CE, CLK, CE
COMP8BIT

U103
COREGen Module
CE, CLK, CE
COMP16BIT

U104
COREGen Module
CE, SCLR
COUNT_8BIT

U105
COREGen Module
CE, SCLR
COUNT_8BIT

U107
COREGen Module
CE, SCLR
COUNT_8BIT

COUNT_8BIT

U102
COREGen Module
CE, SCLR, CE
COUNTER8BIT

U108
COREGen Module
CE, SCLR
COUNTER16BIT

U109
COREGen Module
CE, SCLR
COUNT_8BIT

U110
COREGen Module
CE, SCLR
COMP_FIXED_8BIT

8 BIT QA O/P

OBUF
LOC=P78

OBUF
LOC=P74

OBUF
LOC=P71

OBUF
LOC=P68

OBUF
LOC=P67

OBUF
LOC=P64

OBUF
LOC=P63

OBUF
LOC=P65

8 BIT QA O/P

OBUF
LOC=P116

OBUF
LOC=P117

OBUF
LOC=P6

OBUF
LOC=P10

OBUF
LOC=P39

OBUF
LOC=P55

OBUF
LOC=P46

OBUF
LOC=P27

OBUF
LOC=P31

O/P TR_EN_OUT & TR SIGNALS FROM ADC_CONT S/MC

Heriot-watt University
EPS-EECE
Edinburgh EH14 4AS
Date Last Modified: 3/16/05

Xilinx: Local Gate Control
Sheet: PAGE 3
Date: 3/14/05
Appendix C. Circuit Diagrams

COUNTER FOR TR PULSE WHEN HIGH (14.88us).

ADC 8 BIT OUTPUTS

LOC=P118
LOC=P114
LOC=P110
LOC=P102
LOC=P107
LOC=P103
LOC=P99
LOC=P95

EXTERNAL SELECT CONTROL INPUT

LOC=P28

ADC ENABLE O/P
Appendix C. Circuit Diagrams

MUX. UNIT FOR EITHER EXTERNAL SELECT RATE OR INTERNAL BASED SELECT RATE

RESETTING THE GLOB_RI FOR EACH TRACKING INPUT

LATCHING UP THE SEL_RATE[2:0] FROM RESETTING OF GLOB_RI
Appendix C: Circuit Diagrams

COUNTER A: 1600 counts = 200us

COUNTER B: 400 counts = 50us

COUNTER C: 400 counts = 50us

CLK RUNNING AT 8 MHZ
APPENDIX D

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APPENDIX E

List of Author’s Publications


Abstract - This paper presents an Active Voltage Control technique, for series connected freewheel diodes in bridge legs, which suppresses the oscillation due to diode snap recovery, and clamps the overshoot sustained during reverse recovery. The need to utilise passive snubbers with this active voltage control technique to overcome the shortcoming of the active clamping, is analysed. This technique allows active balancing of the reverse voltage sharing among series connected free-wheel diodes. Experimental results are presented for the suppression of the oscillation seen by the freewheeling diodes and the active clamping of the overshoot voltage with and without passive snubbers.